Sem IV ET CBGS AE 2

1915/14

QP Code : NP-19691

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No. 1** is **Compulsory.**
(2) Solve any **three** questions from remaining **five** questions.
(3) **Figures** to the right indicate **full marks.**
(4) Assume suitable data if necessary and mention the same in answer sheet.

1. Solve any **five** **20**
   (a) Compare ideal and practical Op Amp.
   (b) Consider a BJT has parameters f_T = 500 MHz at Ic = 1 mA, β = 100 and Cμ = 0.3 pF. Calculate bandwidth f_β and capacitance Cπ of a BJT.
   (c) What is cross-over disortion in power Amplifier. How it is overcome?
   (d) Which type of biasing technique is used to bias Integrated Circuit and why?
   (e) Find output voltage of differential amplifier if its differential gain Ad = 100, common mode gain Ac = 0.1 and input voltage are $V_1 = 2 + 0.55 \sin\omega t$ and $V_2 = 0.5 - 0.005 \sin\omega t$.
   (f) Explain line regulation and load regulation of voltage regulator. Draw load and line regulation characteristics of ideal and practical voltage regulator.

2. (a) For the circuit shown in Fig 2a, the parameters are R_s = 0.1 kΩ, R_1 = 20kΩ, R_2 = 2.2 kΩ, R_E = 0.1 KΩ, Cc = 47 μf, and Vcc = 10V. The transistor parameters are : $V_{BE(ON)}$ = 0.7V, β = 200, and VA = ∞. **10**
      (i) Derive expression for lower cut-off frequency (or time constant) due to coupling capacitor Cc,
      (ii) Determine lower cut off frequency and midband voltage gain.

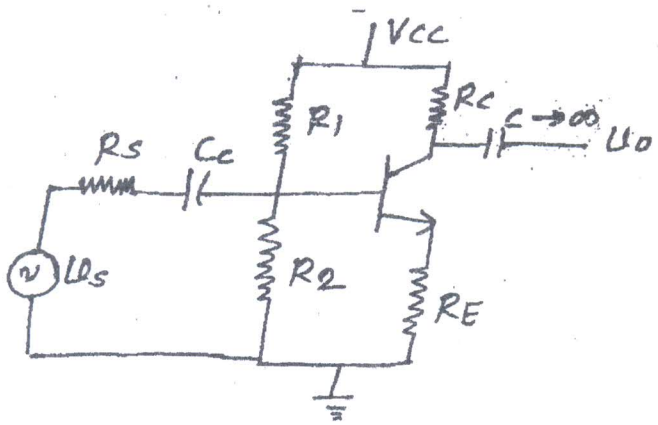

Fig 2a

2.. (b) For the circuit shown Fig.2b, the transistor parameters are : Kn = 1mA/V², V_{TN} = 0.8V, $\lambda = 0$, Cgs = 2pF, and cgd = 0.2pF. Determine 10

(i) Miller capacitance
(ii) The upper 3dB (high cut-off) frequency
(iii) The mid band voltage gain

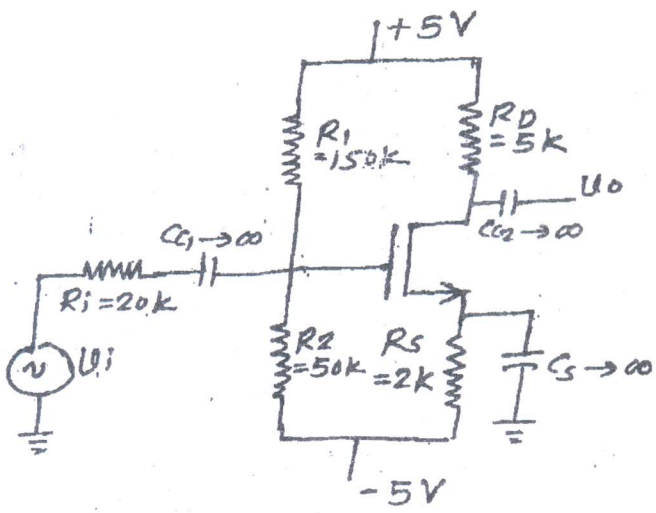

Fig.2b

3. (a) For the circuit shown in Fig.3a, find overall midband voltage gain and capacitors Cc_1 and Cc_2 such that the 3dB frequencies associated with each stage are equal. Assume BJT have parameters : $V_{BE(ON)}$ = 0.7 V, $\beta = 200$, and VA = ∞. 10

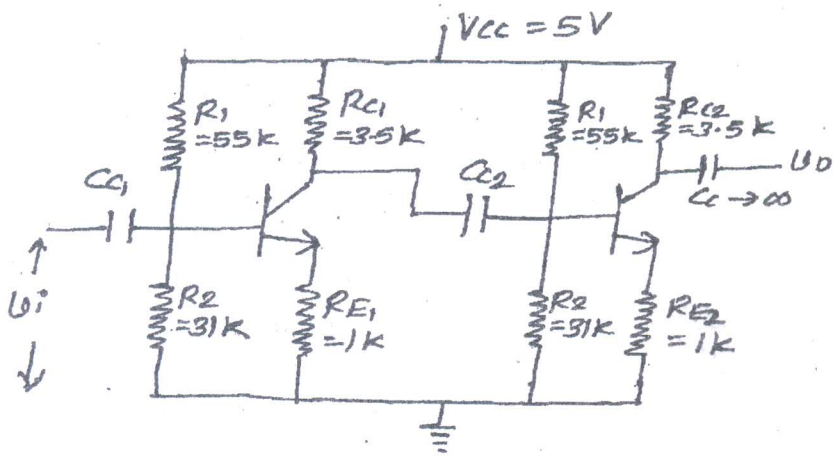

Fig.3a

3. (b) For the differential amplifier shown in Fig 3b, derive expression for differential voltage gain, common-mode voltage gain and CMRR. 10

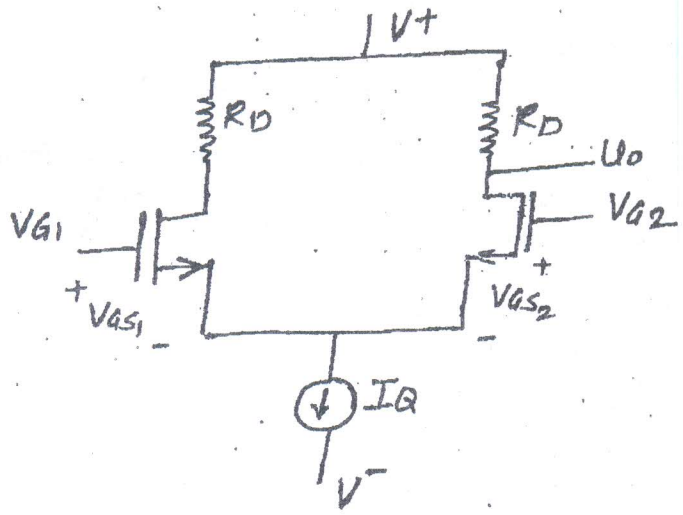

Fig 3b

4. (a) The transistor parameters for the circuit shown in Fig 4a are $\beta = 100$, $V_{BE(ON)} = 0.7V$, and $VA = \infty$. 10

(i) Determine R_B such that $I_E = 150\ \mu A$.

(ii) Find Ad, Acm and CMRR for one sided output at υ_{02}.

(iii) Determine the differential and common-mode input resistances.

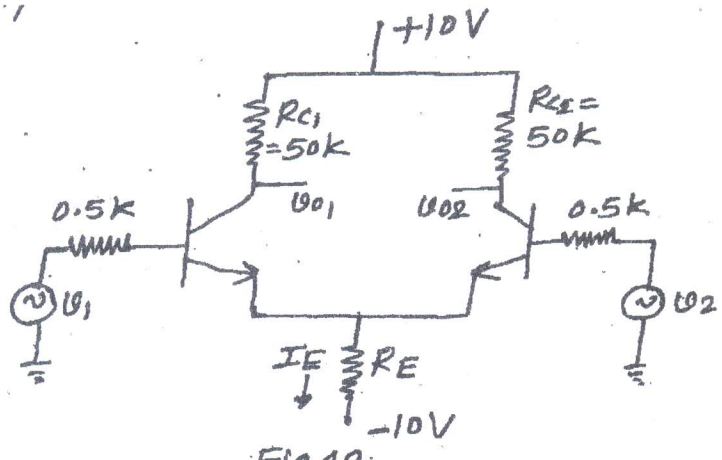

Fig 4a

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