SEM VII COMP OOSE 13/5/14

QP Code : **MV-18077**

(3 hours) **[Total Marks : 100**

N.B. (1) Question no. **1** is **compulsory**.
(2) **Attempt** any **four** out of remaining **six** questions.
(3) **Draw** neat and clean **diagrams**.
(4) State your assumptions **clearly**.
(5) **Illustrate** with suitable examples.

1. (a) Develop the class diagram for the following scenario :– **10**
School has one or more departments. Department offers one or more subjects. A particular subject will be offered by only one department. Department has instructors and instructors can work for one or more departments. Student can enrol in up to 5 subjects in a school. Instructor can teach up to 3 subjects. The same subject can be taught by the different instructors. Students can be enrolled in more than one school. **10**
(b) Realise any of the many-to-many association between two classes of above example using Java code. **10**
10

2. (a) Explain function point Analysis and its relationship with LOC and COCOMO.
(b) Explain the methods of identifying objects for the problem statement. **10**
10

3. (a) Define Design Patterns. Classify Design Patterns.
(b) Explain the process of CMM. **10**
10

4. (a) Elaborate on User Acceptance Testing.
(b) Explain the identification of subsystems and interfaces. **10**
10

5. (a) Explain th various characteristics of the requirements.
(b) Explain software Configuration item identification. **10**
10

6. (a) Explain and compare FTR and walk through.
(b) Explain the process of debugging. **20**

7. Write short notes on (any **two**) :–
(a) Version Control and Change Control
(b) Architectural Styles
(c) Risk management
(d) Agile process.

Con. 9596-14.

P.V.P.P. COLLEGE OF ENGG. SION, MUMBAI - 22. 13 MAY 2014

T.E sem VII Comp. 20/5/14
Subj: AMP.

QP Code : MV-18124

(3 Hours) **[Total Marks : 100**

N.B.:

1. Q. 1 is compulsory.
2. Answer any four questions from remaining questions.
3. Assume suitable data if necessary.
4. Figures to the right indicate full marks.

Q.1.	a)	Explain instruction pairing on Pentium processor.	05
	b)	Explain control and structural hazards with respect to superscalar processor architecture.	05
	c)	Write short note on RISC evaluation.	05
	d)	Explain IA 64 Itanium processor architecture in brief.	05
Q.2.	a)	What is descriptor? Explain Code and Data segment descriptor with neat diagram.	10
	b)	Explain protection mechanism implemented on 80386DX..	10
Q.3.	a)	Explain Integer pipeline of Pentium processor.	10
	b)	Explain Pentium processor architecture with block diagram.	10
Q.4.	a)	Explain Pentium II software changes in detail.	10
	b)	Explain branch prediction logic implemented on Pentium processor.	10
Q.5.	a)	Explain cache/MMU organization of SuperSPARC processor.	10
	b)	Explain, in detail, register file of SPARC processor.	10
Q.6.	a)	Explain the features of USB bus. Also, explain features of ISA bus.	10
	b)	Write short note on I. ATA II. SCSI	10
Q.7.	Write short note on		
	a)	Cache memory organization	05
	b)	Pentium IV processor	05
	c)	Systolic architecture	05
	d)	Operating modes of 80386	05

Con. 10849-14.