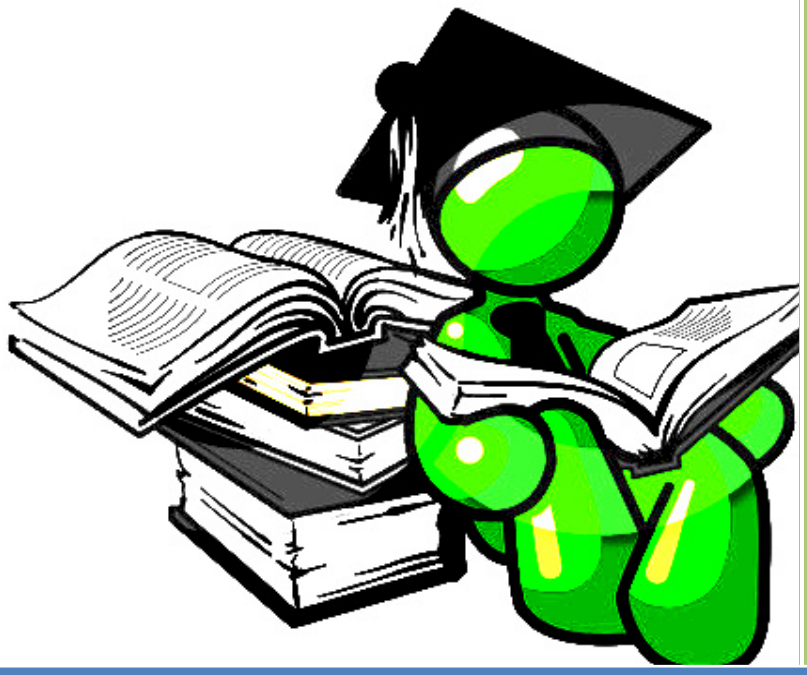
FH 2015



ACADEMIC BOOK

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
COLLEGE OF ENGINEERING
SINCERITY SACRIFICE
SYSTEM
1990
Empower The Knowledge

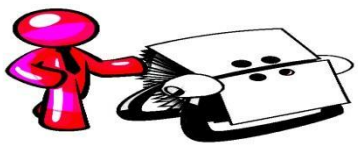
SEMESRTER VIII

BE-ELECTRONICS

FH 2015

ACADEMIC BOOK

INDEX



Department of Electronics Engineering
FH OF 2014 -SEM – IV /VI / VIII

Rules and Regulations

College Timings:

The college timing is from 8:45 AM to 4:45 PM .The students must follow the college timing.

Academic calendar and Time table:

The details of academic curriculum and activities are mentioned in the academic book. The students are required to strictly follow the class Time table and academic calendar.

Attendance:

All students are hereby informed that attendance for lectures/practical/tutorials is compulsory. Mumbai University does not allow students to appear for examination if their attendance is less than 75%.But for the good academic performance of the students, the department expects 100 % attendance in theory and practical separately.

Defaulters:

Defaulters list will be displayed monthly. The defaulter students are required to bring their parents/guardians within four days after the display of defaulters list. If students remain defaulter consistently he/she has to face the consequences as laid by the Mumbai University.

Assembly/prayer:

The Assembly /Prayer starts at 8:50 AM. The student must remain present in their respective classes for the prayer. The students reporting the college late will be treated as late comers and their attendance will be noted in the separate register. After three late marks the students are expected to bring their parents /guardians to the college.

Identity card:
Student must wear ID during college hours in the campus.

Mobile Phone:
Use of cell phone is strictly prohibited in the college premises.

Examination:
As per the university norms, there will be two term test i.e Mid Term test and End Term test in the semester which is an integral part of Internal Assessment for every subject. Both the examination will be based on 40 % and 70 % of theory syllabus respectively for each subject and will be conducted as per the dates mentioned in the academic calendar. Attendance for both internal examination IS COMPULSORY .As per the university norms, no retest will be conducted under any circumstances. Separate passing heads is compulsory for internal and external examination for individual subjects. If the student fails in any of the exam he/she has to reappear in the concerned subject after the declaration of the result.

Practicals/tutorials/Assignments:
The Student should compulsory bring their rough and fair journal for the concerned subject for every practical and tutorials and get it checked regularly. Failing to do so, they will not be allowed for the practical. The Assignments for every subject should be submitted on regular basis.

The student must abide by the above mentioned rules and regulations laid down by the department for their better and brighter future.

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FH 2015

ROBOTICS AND AUTOMATION

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY SACRIFICE
SYSTEM 1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mrs.S.N.DESHPANDE

Subject Plan

GROUP NAME : AUTOMATION
COURSE TITLE : ROBOTICS AND AUTOMATION **COURSE CODE : -** **SEM : VIII (FH 2015)**
1. PRE-REQUISITE : Concept of Matrix Algebra, Fundamentals of Image Processing,Fundamentals of Controllers.

RATIONALE

This course in automation group aims to introduce the student to the basics of automation as a foundation course for industrial robots

OBJECTIVES :

1. To introduce the students to the fundamentals of analysis and the control of industrial robots.
2. To recognize objects in the workspace and determine their positions and orientations so that they can be successfully manipulated by the robots.
3. To introduce students to hardware components for automation like Programmable Logic Controllers.

OUTCOME :

1. Students will get acquainted with a range of robots from one axis to six axis.
2. With the effective use of robotic vision, students will get valuable information that can be used to automate the manipulation of objects.

3. They would be able to use techniques, skills and modern engineering tools necessary for Robotics and Automation practice.
4. Students can apply their knowledge in industrial applications.
5. The student should become confident enough to evaluate, choose and incorporate robots and PLC in engineering systems.

LEARNING RESOURCES: -

RECOMMENDED BOOKS: -

Text Book :

1. Robert Shilling, Fundamentals of Robotics-Analysis and control, Prentice Hall of India
2. Fu, Gonzales and Lee, Robotics, McGraw Hill
3. J.J, Craig, Introduction to Robotics, Pearson Education
4. Curtis D. Johnson, Process Control Instrumentation Technology, PHI Publication, Eighth Edition

Reference Books :

5. Staughard, Robotics and AI, Prentice Hall of India
6. Grover, Wiess, Nagel, Oderey, "Industrial Robotics", McGraw Hill
7. Walfram Stdder, Robotics and Mechatronics,
8. Niku, Introduction to Robotics, Pearson Education
9. Klafter, Chmielewski, Negin, Robot Engineering, Prentice Hall of India
10. Mittal, Nagrath, Robotics and Control, Tata McGraw Hill publications
11. George L Balten Jr., Programmable Controllers , Tata McGraw

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapterwise Question Bank

Evaluation :

Theory Exam	100 M

Internal assessment:-. The average marks of Mid-term test (20 M) & End-term test (20 M) will be considered as final IA marks for T/W(10M)	20 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Atleast 06 experiments based on the entire syllabus

Expt. No.	Name of the Experiments
1	PROGRAM FOR FIBONACCI SERIES
2	COMPUTE MOMENTS OF FOREGROUND REGION OF A BINARY IMAGE.
3	COMPUTE THE RUN LENGTH ENCODING OF A BINARY IMAGE.
4	DIRECT KINEMATICS OF RHINO XR3 ROBOT.
5	INVERSE KINEMATIC ANALYSIS OF A FIVE AXIS ARTICULATED RHINO XR3 ROBOT ARM.
6	TEMPLATE MATCHING.
7	INVERSE KINEMATICS OF FOUR AXES SCARA ROBOT.
8	DIRECT KINEMATICS OF FOUR AXES SCARA ROBOT.

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 1

Chapter Name : Introduction to Robotics

Approximate Time Needed : 05 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Automation and Robots
2	Classification
3	Application
4	Specification
5	Notations

Objectives:

1. To define scope of Robotics and Automation.
2. To give an idea of some of the principal areas in which it is applied.
3. To discuss principal approaches used in Robotics and Automation.
4. Robotics and Automation fundamentals.

Lesson Outcome:

Students will able to

1. Scope of Robotics and Automation.
2. Principle areas in which it is applied.

3. Robotics and Automation fundamentals

Model Questions:

DEC 2013

1. Classification of Robots [5]

Dec 2011

1. Why is SCARA arm more ideal for assembly application?

June 2011

1 . Compare hard and soft automation. State advantages and disadvantages of both.

DEC 2010

1 . Explain the following terms related to robot-DOF, Reach, Stroke, Tool orientation, Precision, Accuracy, Repeatability, Load carrying capacity, Speed, work envelop.

June 2010

1. How are robots classified?

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 2

Chapter Name : Direct Kinematics FIR DIGITAL FILTERS

Approximate Time Needed : 12 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
6	Dot and cross products,
7	Co-ordinate frames,
8	Co-ordinate frames,
9	Rotations,
10	Rotations,
11	Homogeneous Co-ordinates,
12	Homogeneous Co-ordinates,
13	Link co-ordinates,
14	Link co-ordinates,
15	Arm equation ((Three axis, Four axis, and Five axis robots)

16	Arm equation ((Three axis, Four axis, and Five axis robots)
17	Arm equation ((Three axis, Four axis, and Five axis robots)

Objectives:

1. To understand the fundamentals of robotics.
2. To learn the Co-ordinate frames.
3. To study applications of Arm equation

Lesson Outcomes:

The student will be able to

1. Fundamentals of robotics.
2. Significance of the Co-ordinate frames.
3. Arm equation and its application.

Model Questions:

June2010

1. Derive the general link co-ordinate transformation matrix $T_K{}^{K-1}$
2. Using D-H algorithm, perform direct kinematic analysis of 5 axis RHINO XR3 robot.

Dec 2010

3. Explain D-H algorithm. Develop D.K. analysis of 4 axis SCARA robot.

June 2011

4. Define kinematic parameters. What is soft home configuration?
5. Apply D-H algorithm for SCARA robot and construct a link-coordinate diagram.
6. Compute arm matrix for the SCARA robot.
7. Obtain Direct kinematic solution of three axis planer articulated robot arm

Dec 2011

8. Why inverse kinematics problem is not unique and direct kinematics problem is unique.
9. What are the considerations for applying DH algorithm? Explain the Direct kinematic solution for three axis planar robot.

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 3

Chapter Name: Inverse Kinematics & Workspace Analysis

Approximate Time Needed : 09 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
18	1 General properties of solutions,
19	Tool configuration,
20	Inverse Kinematics of Three axis,
21	Four axis and
22	Five axis robots
23	Workspace analysis of Four axis and Five axis robots
24	Workspace analysis of Four axis and Five axis robots
25	Work envelope,
26	Workspace fixtures.

Objectives:

1. To understand the principle of Inverse Kinematics.
2. To learn Workspace analysis.
3. To study different Work envelops.

Lesson Outcomes

The student will learn

1. Inverse Kinematics
2. Workspace analysis
3. Work envelop

Model Questions:

June 2010

1. Compute the joint variable vector q = $[q_1, q_2, q_3, q_4]^T$ for the following tool configuration vector of SCARA. W(q)=$[203, 662.7, 557, 0, 0, -1.649]^T$
2. Describe the solution of inverse kinematic problem of a 2-axis planar robot.
3. Explain work space analysis of 5-axis RHINO-XP3 robot by finding the maximum and minimum bounds.

Dec 2010

4. Explain composite rotation matrix (CRM) algorithm.
5. Discuss work envelop of 4-axis SCARA robot.
6. Develop IK analysis of 2-axis planar articulated robot.
7. Compare joint variable vector q = $[q_1, q_2, q_3, q_4]^T$ for the following TCV of SCARA. W(q) = $[203.43, 662.7, 557, 0, 0, -1.649]^T$

June 2011

8. Explain the properties of inverse kinematic solution.
9. Explain the screw transformation. Show that the inverse of a screw transformation is again a screw transformation.
10. Define Tool Configuration vector. Show how to obtain tool roll angle. What are the advantages/disadvantages of numerical approach and analytical approach to solve the inverse kinematics problems?

Dec 2011

11. Differentiate between direct kinematics and inverse kinematics problems.

12. Obtain the inverse kinematics solution of the 4 axis Adept-1 SCARA robot with its IK algorithm starting from the arm matrix. Explain each joint variable computation in brief.
13. Define total work envelop, joint space work envelop, dexterous work envelope with their relevant formulas and illustrate these for any one robot with a neat sketch.
14. Derive the three fundamental matrices R1(θ), R2(θ), R3(θ) with the help of neat sketches.

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 4

Chapter Name : Trajectory Planning and Task Planning

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
27	Trajectory planning, Pick and place operations, Continuous path motion,
28	Interpolated motion, Straight-line motion.
29	Task level programming,
30	Uncertainty Configuration space,
31	Gross motion planning, Grasp planning,
32	Fine-motion Planning,
33	Simulation of Planar motion,
34	Source and goal scenes, Task planner simulation

Objectives:

. Students should know :

1. Trajectory Planning
2. Task Planning

Lesson Outcomes

Student will do

1. Trajectory Planning

2. Task Planning

Model Questions:

June2010

1. Explain the process of linear interpolation with parabolic Blends.
2. Explain the effect of moment of inertia on the dynamic performance of a robot.
3. Explain the PNP motion trajectory in details.
4. Explain bounded deviation algorithm for achieving straight line motion.

Dec 2010

5. Explain how straight line motion can be obtained using an articulated robot.
6. Explain linear interpolation with parabolic blends. Discuss its advantages over piecewise linear interpolation.
7. Explain the effect of moment of inertia on the dynamic performance of a robot.

June 2011

8. Define following terms tool path, Tool trajectory, DOF
9. Explain the 4 point minimal PNP trajectory for pick and place of objects by using a robot manipulator.
10. What is a GVD? Sketch all the GVD's resulting due to the basic interactions of the obstacles . Derive the necessary equations.

Dec 2011

11. What is trajectory planning? Explain in brief How continuous motion path trajectory is planned .
12. What is robot task planner? Explain in brief with the help of a block diagram.

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 5

Chapter Name : **Robot Vision**

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
35	Robot Vision Image representation
36	Template matching, Polyhedral objects
37	Shape analysis, Segmentation,
38	Iterative processing,
39	Perspective transformation
40	Structured Illumination

Objectives:

Fundamentals of Robot Vision

Outcomes:

The students will learn

Fundamentals of Robot Vision

Model Questions:

June 2010

1. Explain the principle and applications of edge detection techniques using gray scale image.

Dec 2010

2.

0	0	1	1	0	0
1	1	1	1	1	1
0	0	1	1	0	0

For the above image, calculate area, centroid, first order moments, second order moments, central moments and principal angle.

3. Discuss edge detection technique. Explain the significance of edge threshold.

June 2011

4. Explain the shrink and swell operators with an example. How are they applied? List all the properties of these operators.

Dec 2011

5. Compare the relative merits and demerits of different structured illumination techniques.

Chapterwise Plan

Subject Title: Robotics and Automation

Chapter No. : 6

Chapter Name : : **Programmable Logic Controller**

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
41	system – symbols used – relays and PLC Software Functions,
42	logic functions – OR, AND, Comparator,
43	Counters review, PLC Design, PLC Operation,
44	Programming of PLCs Discrete-State Process Control,
45	Relay Controllers background
46	hardwired control system definition, Ladder Diagram Elements and examples,
47	Relay Sequencers,
48	Evolutions of PLCs , Block advantages of Programmable Logic Controller (PLC),diagram of PLC

Objectives:

To study

1. Fundamentals of Programmable Logic Controller.

Lesson Outcomes:

The student will learn

1. Fundamentals of Programmable Logic Controller

Model Questions:

June 2011

1. Draw symbols of input and output devices and the switches used in ladder diagram.
2. Explain in details block diagram of PLC (programmable Logic Controller). Hence write ladder diagram programs to implement Logic Functions AND, OR, NOT, NAND, NOR
3. Write specifications of PLC
4. Write industrial applications of PLC

Dec 2011

5. What are advantages of PLC. List examples of PLCs and their manufacturers.
6. Explain structure of Timer and Counter Functions. Hence give one example of each.
7. List programming languages used for PLC. Explain any one language in brief.

Assignments

ASSIGNMENT 1 (DATE : 9th FEB 2015)

Write short notes on –

1. Screw transformation
2. Robot programming
3. Robot classification
4. Work space fixtures
5. Robot specifications

Q1. a) Explain and draw basic four steps for transferring Frame k-1 to frame k **5 marks**

Q2. a). What is the inverse kinematics problem and state different methods to solve inverse kinematics problem in brief. **10 marks**

b) Explain the conditions for the existence of the Inverse Kinematics solutions. **4 marks**

c) Define total workenvelope, joint space work envelope, dexterous work envelope ,with their relevant formulas and with a neat sketch. **6 marks**

Q3. a). Obtain the Inverse Kinematics solution of the 4 axis Adept - 1 SCARA robot with its IK algorithm starting from the arm matrix. Explain each joint variable computation in brief. **10 marks**

b) Find a single composite transformation matrix T (T_{YPR} only with numeric values) which maps the tool coordinates *M* into the wrist coordinates *F* following the sequence of rotations of *M* frame about the unit vectors of *F* . **10 marks**

(c)Explain the following terms, Tool path, Tool trajectory, DOF,TCV, TWE. [05]

(d)Write any three points why inverse kinematic solution is not unique [05]

Q2.(a)Using DH algorithm perform direct kinematic analysis of four axis ADAPT-1 SCARA robot. [10]

(b) Compute the joint variable vector $q = [q_1, q_2, q_3, q_4]^T$ for the following tool configuration vector of

SCARA. $w(q) = [692.82, 25, 527, 0, 0, -1.6487]^T$, where

$a_1 = 425mm, a_2 = 375mm, a_3 = 0, a_4 = 0$, and $d_1 = 877mm, d_2 = 0, d_3 = q_3, d_4 = 200mm.$ [10]

Q3.(a)Discuss Inverse kinematic analysis of five axis Microbot α-II Articulated Robot arm. [10]

(b) Find the composite rotation matrix by rotating the tool about the fixed axis of F frame, with a yaw of $\left(\frac{\pi}{2}\right)$, followed by a pitch of $\left(\frac{-\pi}{2}\right)$ and finally a roll of $\left(\frac{\pi}{2}\right)$ radians. If $(p)^M = (0, 0, 0.6)^T$ $Find$ $[p]^F$ [10]

Q.6. a)Explain workspace analysis of 5 axis Rhino XR-3 Robot arm **10 marks**

ASSIGNMENT 2 (DATE : 13th March 2015)

b) Explain the basic steps involved in bounded deviation algorithm for straight line motion . **5 marks**

c) Define Pixel function, Shrink Operator and Swell operator **5 marks**

d) What are the advantages & disadvantages of PLC system **5 marks**

Q4.(a) Explain how straight line motion can be obtained using articulated robot.

[10]

(b)Differentiate between path and trajectory. Define SDF. Explain in brief how continuous motion path trajectory is generated. [10]

Q1. (a)Explain the process of edge detection. [05]

(b)Explain programming languages used for PLC, explain any one language in brief. [05]

Q4.(a) Explain how straight line motion can be obtained using articulated robot.

[10]

(b)Differentiate between path and trajectory. Define SDF. Explain in brief how continuous motion path trajectory is generated. [10]

Q5.(a) Explain shrink and swell operators. How does swell operator help in image smoothening, explain with an example. [10]

(b)What are advantages of PLC's explain with examples, also state the specifications of PLC with Industrial application and manufacturer. [10]

Q6.(a)Compare traditional ladder diagram and PLC ladder diagram with examples.

[10]

(b) Write short note on corner point detection. [10]

Q.4. a) Explain with example normalization of the performance index for removing the effects of average light intensity. 10 marks

b)What are area descriptors? What are its advantages over line descriptors ? 10 marks

Q.5. a) Explain how the chain code of a boundary is constructed? 10 marks

b) Explain the template matching algorithmfor object recognition. 10 marks

b)Write a PLC ladder logic programme for 4 junction traffic light controller 10 marks

Write short notes on –

1. Shrink and Swell operators
2. Template matching
3. Shape analysis of objects
4. Gross and fine motion planning
5. Reach and stroke of robot
6. Perspective Transformation

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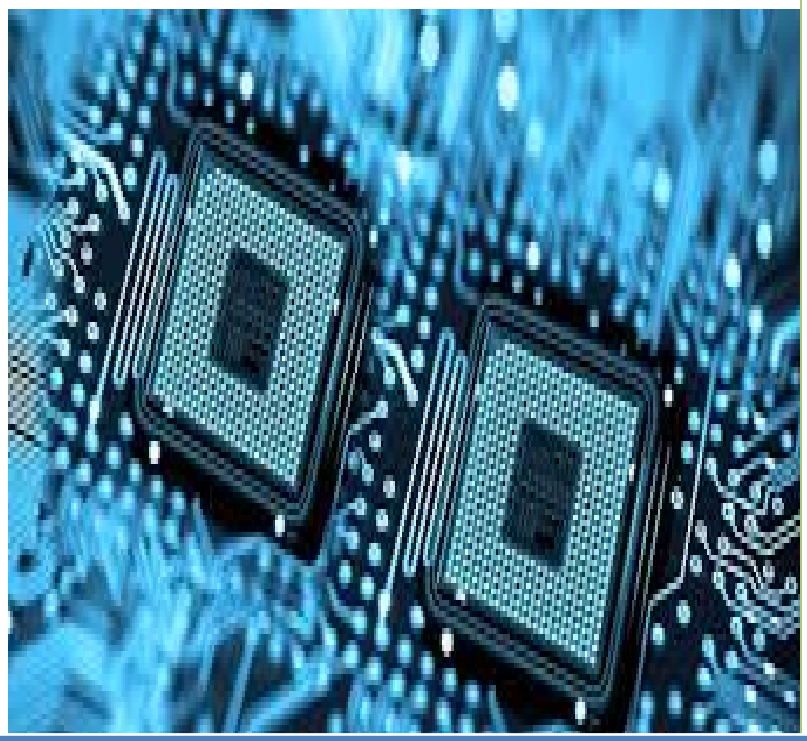

FH 2015

ADVANCED VLSI DESIGN

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
COLLEGE OF ENGINEERING
SINCERITY
SACRIFICE
SYSTEM
1990
Empower The Knowledge

Mrs.DEEPALI BHOSALE

Subject Plan

GROUP NAME : Integrated Circuits
COURSE TITLE : AVLSI Design **SEM : VI (FH 2015)**
PRE-REQUISITE : **DSD-I,DSD-II, BEC and VLSI Design.**

RATIONALE

This subject covers several aspects of digital circuit design. Starting with device equations, we will delve into several areas of digital circuit design, including recent changes in circuit design styles and future trends in digital circuit design. We will cover different design styles, memory design, leakage power control and exploitation, board level design concepts, and clocking and dynamic compensation of circuit characteristics.

The goal of the subject is to take you through a tour of the issues a typical circuit designer in industry deals with, and the design techniques they utilize. The focus is on custom digital VLSI design. At the end of this course, students would have an understanding of the analysis techniques and tools that are required for a VLSI circuit designer to effectively function in today's industry.

OBJECTIVES :

2. To understand Parameters related to interconnect , Different wire models
3. To learn CMOS amplifiers, Sample and hold circuit .
4. Understanding of Clock generation and distribution.
5. Clocking systems in different phases
6. To understand concept of Low power design consideration
7. To study circuits like Logic arrays
8. To learn CMOS memory structures
9. Use of CMOS VLSI for Arithmetic circuits
10. Solutions for charge sharing
11. Understand Pipelining

OUTCOME :

6. Students will understand What are the various parameters (resistance, capacitance & inductance) associated with the interconnects in an IC, Different wire models
7. Students will learn CMOS amplifiers
8. Students will be Able to define What is charge sharing and problems related to charge sharing
9. How a system can be clocked using different phases
10. What is pipelining and advantages
11. Designing the various adders using CMOS
12. Designing the Static and dynamic RAM structures
13. Designing different ROM cells
14. What is clock skew, problems related to clock skew and propagation delay
15. How to obtain a low power design circuit
16. Design of various CMOS amplifiers
17. Design of sample and hold circuits

LEARNING RESOURCES: -

RECOMMENDED BOOKS: -

1. Neil H.E. Weste, Kamran Eshraghian, Principles of CMOS VLSI Design: A system perspective, Addison Wesley publication.
2. Fabricius, Eugene D, Introduction to VlSI Design. TMH
3. P.R. Gray & R.G. Meyer, Analysis and design of analog integrated circuits, John Wiley
4. John P. Uyemura, Introduction to VLSI Circuits and systems, John Wiley & sons.
5. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, Second Ed., MGH
6. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall
7. D.Razavi, Design of Analog CMOS circuits, McGraw Hill

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapterwise Question Bank

Evaluation :

Theory Exam	100 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Expt. No.	Name of the Experiments
1	To simulate resistance and capacitance estimation
2	To simulate CMOS amplifiers
3	To simulate the layout of DRAM cell.
4	To simulate the layout of basic 6T SRAM Cell
5	To simulate the layout of basic 6T SRAM Cell
6	To simulate the layout of D-latch
7	To simulate the layout of Ripple carry adder.
8	To simulate the layout of Half adder.
9	To simulate the layout of Full adder.
10	To simulate differential amplifiers

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 1

Chapter Name : WIRE INTERCONNECT FOR CIRCUIT SIMULATION

Approximate Time Needed : 07hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Interconnect parameters (Capacitance, Resistance and Inductance) their effect on circuit performance.
2	Electrical wire models (ideal, lumped).
3	Electrical wire models (lumped rc, distributed rc and transmission line).
4	Switching characteristics, transistor sizing
5	Sizing routing conductors, charge sharing and reliability issues.
6	Numericals on each subtopic.
7	Numericals on each subtopic.

Objectives:

1. To Understand the Parameters related to interconnect
2. To Learn Different wire models.
3. Switching characteristics and sizing of transistor
4. Study Charge sharing

Lesson Outcome:

Students will able to

1. Learn what are the various parameters (resistance,capacitance&inductance) associated with the interconnects in an IC
2. Understand what are the different ways in which wires can be modeled
3. Understand how a transistor can be sized, advantages and disadvantages of transistor sizing
4. Understand charge sharing and problems related to charge sharing

Model Questions:

JUNE 2014

1. Give & expalin the routing capacitance with fringing field effect 5
2. Explain in detail sizing of routing conductor with respect to metal migration and ground bounce / power supply drop. 10

DEC 2013

1. If the width and length of the interconnect is reduced by 30%, then the propagation delayf an interconnect will increase or decrease, by how much %? 5
2. What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100pF of on-chip load to satisfy the metal-migration consideration (JAL =0.5 mA/μm)? What is the groumd bounce with chosen conductor size? The module is 500 μm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1ns.
   (Assume sheet resistance of wire = 0.05Ω/sq) . 10
3. Reliability issues in CMOS circuits 5

May 2013

1. Expalin electromigration effect in an Inter connect
2. Give and expalin the capacitances associated with an interconnect and expalin how

propagation of signal depends upon the distributed RC effect. 10

Dec 2012

1. What are PVT variations and how does PVT affect integrated circuit. 5
2. What is Elmore delay model. What is the effect of interconnect parasitics on delay? How delay can be reduced? 10
3. Metal migration in interconnect. 5

June 2012

1. What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100pF of on-chip load to satisfy the metal-migration consideration (JAL =0.5 mA/μm)? What is the groumd bounce with chosen conductor size? The module is 500 μm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1ns. (Assume sheet resistance of wire = 0.05Ω/sq) . 10
2. Expalin Metal migration in interconnect. 5
3. If the width and length of the interconnect is reduced by 30%, then the propagation delay of an interconnect will increase or decrease, by how much %? 5
4. Reliability issues in CMOS circuits 5

DEC 2011

1. An nFET with L=0.5 μm is built in a process where Kn' = 100μA/V2 and Vtn=0.7V. The gate to source voltage is set to a value of VGSn =VDD =3.3V.Calculate the required channel width to obtain a resistance of Rn =950Ω (use value of =1) 5
2. What are the parasitic elements of interconnect wire and how it affects electrical behavior of the circuit. 10
3. Explain modeling of RC delay of interconnect wire using distributed RC model. How this delay can be reduced? 10

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 2

Chapter Name : SEQUENTIAL LOGIC CIRCUITS DESIGN

Approximate Time Needed : 9 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
8	Clocked systems Single phase, Two phase and four phase clocking.
9	Clocked CMOS circuits
10	Dynamic CMOS circuits
11	Solutions for charge sharing
12	VLSI sequential system components such as Flip Flops.
13	Static latches
14	Dynamic latches
15	Registers and Pipelining concepts
16	Discussion on university question papers.

Objectives:

1. To make the students understand the concept of Clocking systems in different phases
2. Learn Dynamic CMOS circuits
3. Find Solutions for charge sharing
4. To understand Various sequential circuits
5. To understand Pipelining

Lesson Outcomes:

The student will be able to

1. Understand how a system can be clocked using different phases
2. Realize Various dynamic circuits
3. Understand How charge sharing problem can be overcome
4. Design Flip flops, latches, registers
5. Learn pipelining and its advantages

Model Questions:

JUNE 2014

1. Give various important parameters affecting switching performance of CMOS inverter. Suggest methods to improve it. 10
2. Give and explain single phase clock system and explain its drawback. 10

DEC 2013

Give and explain single phase clock system and explain its drawback. 10

MAY 2013

1. Give and explain single phase clock system and explain its drawback. 10
2. Pipelined system. 5

DEC 2012

1. Discuss to concept of charge sharing and explain how it affects reliability of integrated circuit. 10
2. Give and explain single phase clock system and explain its drawback. 10
3. Discuss dynamic CMOS logic. Compare it with static CMOS logic. What is to primary drawback of dynamic CMOS logic. Show to modifications in dynamic CMOS logic to overcome its drawback. 10

JUNE 2012

Give and explain single phase clock system and explain its drawback. 10

DEC 2011

Explain pipelined design concept. 5

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 3

Chapter Name : **ARITHMETIC CIRCUITS IN CMOS VLSI**

Approximate Time Needed : 6 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
17	Dynamic adders.
18	Fast adders.
19	Wide adders
20	Carry look ahead adder
21	Block generate and propagate
22	Carry save and carry skip adder

Objectives:

4. Learn different Arithmetic circuits using CMOS in VLSI

Lesson Outcomes:

The student will be able to

1. Design the various adders using CMOS
2. Design an adder with carry and by skipping the carry

Model Questions:

JUNE 2014

1. Give & expalin carry save adder 5
2. Draw and explain full adder using dual rail complementary pass transistor logic. 10

DEC 2013

Short note on Manchester carry circuit. 5

MAY 2013

1. Draw the circuit using propragate and generate term for 4-bit CLA network, in each of the following :
   (i) nFET logic
   (ii) Pseudo nMOS logic. 10
2. Manchester carry chain circuits and MODL circuit. 7

DEC 2012

1. Show to implementation of four bit carry look ahead adder along with all to Equations 10
2. Draw and expalin Manchester carry out circuit using carry kill bit. Also draw k-input dynamic Manchester carry chain circuits. 10

JUNE 2012

1. Draw and expalin Manchester carry out circuit using carry kill bit. Also draw 4-input dynamic Manchester carry chain circuits. 5

2. Give and explain the drawback with ripple carry adder. Explain 4-bit CLA adder with its carry equations, logical network and write its verilog description. 10
3. Carry save adder. 7

DEC 2011

Implement 4 bit adder using Carry Look Ahead (CLA) principle 10

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 4

Chapter Name : **DESIGN OF MEMORIES & PROGRAMMABLE LOGIC**

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
23	CMOS Memory structures – SRAM design
24	CMOS Memory structures –DRAM design
25	Sense amplifier design - Low power design techniques.
26	ROM Arrays
27	Logic Arrays
28	EPROM, EEPROM
29	Flash cell working.
30	Design of basic 6T SRAM Cell with read and write stability criteria

Objectives:

1. To understand CMOS memory structures
2. To learn Low power design techniques
3. Study different Logic arrays

Lesson Outcomes

1. Designing the Static and dynamic RAM structures
2. Using which technique one can design a low power circuit
3. Designing different ROM cells

Model Questions:

JUNE 2014

1. Sense amplifier 7
2. Floating gate MOSFET. 7
3. Draw three variable- three output PLA and programme it with following functions
   fx= ac+be
   i. Fy= abc+abc
   ii. Fz= ab+ab 10
4. Draw 1T DRAM cell and explain its write, read , hold and refresh operation . 10
5. Write Specification of Row Decoder, Column Decoder and MUX/ DMUX used in 64 * 8 SRAM 5

DEC 2013

1. Expalin programming techniques of EEPROM. 5
2. Explain 4-bit CLA adder with its carry equations, logical network and write its verilog description. 10
3. Draw 6T DRAM cell and explain its operation butter-fly plot . 10

MAY *2013*

1. The storage capacitor in a DRAM has a value of Cs=55fF. The circuitary restricts the capacitor voltage to a value of Vmax= 3.5V; when the access transistor is off , the leakage current of the cell is estimated to be 75nA.
   (i) How many electrons can be stored on Cs ?
   (ii) How many fundamental charge unit q leave the cell in 1 second due to leakage current 10
2. Draw and explain trench capacitor and stacked capacitor structure of DRAM cell. 5
3. EEPROM programming technique . 7

DEC 2012

1. Draw schematic for 6T SRAM cell and explain its stability criteria .Also draw and discuss butter-fly curve . 10
2. Discuss in programming techniques of EEPROM in details. 10
3. DRAM and refresh logic 7

JUNE 2012

1. Explain programming techniques of EEPROM using hot electron and Fowler-Northeim emission. 5
2. Draw 1T DRAM cell and explain its write, read , hold and refresh operation . 10
3. Draw 4 * 4 pseudo-nMOS ROM array cicuitry having stored following data: 0011,1010,1100,0101. Also list the no. Of address pins, data pins and word lines. 10

DEC 2011

1. What is the cell ratio and pull up ratio of 6T SRAM cell.How does these affect the read/write operation. 10
2. Explain cross coupled differential sense amplifier with circuit diagram which is used in SRAM cell. State the advantages over other differential sense amplifiers. 10
3. Explain EEPROM using floating gate NMOSFET. 10
4. Implement the following function using NOR-NOR implementation for a PLA
   (i) Y1= ab+c
   (ii)Y2= c + abc
   (iii) Y3=b+ac 10

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 5

Chapter Name : **TIMING ISSUES & SYSTEM LEVEL PHYSICAL DESIGN**

Approximate Time Needed : 09 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
31	Timing classification, Synchronous timing basics, Clock generation and distribution
32	Clock skew, propagation delay estimation
33	Clock jitter, combined clock skew and clock jitter estimation
34	Synchronous and asynchronous design timing estimations.
35	Crosstalk, Interconnect Scaling
36	Floor planning & Routing
37	I/P & O/P Circuit
38	Power dissipation and consumption
39	Low power Design considerations

Objectives:

To understand

1. Timing classification
2. Crosstalk
3. Floor planning and routing
4. Power dissipation
5. Low power design consideration

Outcomes:

The students will be able to understand

1. What is clock skew, problems related to clock skew and propagation delay
2. Estimation of design timing of various synchronous and asynchronous circuits
3. What is crosstalk, problems and solution related to crosstalk
4. What is floor planning and routing. How it is done and their advantages
5. How to obtain a low power design circuit

Model Questions:

JUNE 2014

1. Give and explain two techniques to improve the minimum frequency requirement of clock signal 5
2. Explain various technique of clock generation. Discuss "H" tree clock distribution. 10
3. Give and explain interconnect scaling. 10
4. Explain need of input protection and give the input protection circuits. 10
5. Low power design consideration 7

DEC 2013

1. Explain the need of interconnect delay model. 5
2. Explain How ESD (electro-static discharge) affect the MOSFET. Give and explain input protection circuits. 10
3. Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10 10
4. Explain various technique of clock generation . Discuss "H" tree clock distribution. What is cross talk in IC's? Explain various methods to reduce it . 10
5. Schmitt trigger input protection circuit. 7
6. Interconnect scaling. 7

MAY 2013

1. Give and explain interconnect scaling with its width, length, thickness and capacitances. 10
2. Draw and Explain Schmitt trigger circuit as a input protection for CMOS. Also explain bi-directional I/O circuits. 10

DEC 2012

1. What do you mean by clock skew and clock jitter. 5
2. State the need of input and output circuit with their neat diagrams. 5
3. Draw and explain clock generation and stabilization network. Also explain how this clock is distributed in integrated circuit. 10
4. Interconnect scaling 7
5. Cross talk in integrated circuits 7

JUNE 2012

1. Explain How ESD (electro-static discharge) affect the MOSFET. Give and explain input protection circuits. 10
2. Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10
3. Explain various technique of clock generation. Discuss "H" tree clock distribution. 10
4. What is cross talk in IC's? Explain various methods to reduce it . 10
5. Low power design consideration. 7

DEC 2011

1. Explain Low power design consideration. 5
2. What are the requirements of a clock signal and list the points to be considered in clock distribution. 10
3. What are the different clocking strategies employed in VLSI systems. Discuss 'H tree' clock distribution in high density CMOS circuits. 10
4. State the need of input and output circuit. Explain with neat diagram the schematic and design considerations for the same. 10
5. What is cross talk in integrated circuits? Explain various methods to reduce it. 10

Chapterwise Plan

Subject Title: AVLSI Design

Chapter No. : 6

Chapter Name : **INTRODUCTION TO ANALOG AND MIXED SIGNAL DESIGN**

Approximate Time Needed : 09 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
40	Building blocks for CMOS amplifiers
41	CMOS operational transconductance amplifiers
42	Frequency compensation schemes.
43	Design of fully differential amplifiers
44	Common mode feedback circuits
45	Switched capacitor circuits
46	Design of sample and hold and comparator circuits
47	To solve university question paper
48	To solve university question paper

Objectives:

To understand

8. CMOS amplifiers
9. Frequency compensation schemes
10. Differential amplifiers
11. Feedback circuits
12. Sample and hold circuit

Lesson Outcomes:

The students will be able to understand

1. Design of various CMOS amplifiers
2. Design of sample and hold circuits

Model Questions:

JUNE 2014

1.	Draw and explain CMOS two-stage OP-AMP.	10
2.	Switch Capacitor amplifier	7

DEC 2013

1.	Explain Switched Capacitor amplifier.	5
2.	Draw and explain CMOS two-stage OP-AMP.	10

MAY 2013

1.	Analog circuit design is difficult as compared to digital circuit design. Justify.	5
2.	Draw and explain CMOS two-stage OP-AMP. Give gain boosting technique.	10
3.	Frequency compensation scheme of CMOS Amplifier.	7

Dec 2012

1.	Analog circuit design is difficult as compared to digital circuit design. Justify.	5
2.	Draw and explain MOS based two stage amplifier. Also discuss how frequency compensation can be achieved.	10
3.	Switch Capacitor circuit	7

June 2012

1.	Explain the need Frequency compensation scheme of CMOS Amplifier	10
2.	Switch Capacitor circuit	7

DEC 2011

1.	Draw analog design octagon and explain its significance.	5
2.	Explain the need of frequency compensation in operational amplifiers.	10

Assignments

ASSIGNMENT 1 (DATE : 9th FEB 2015)

1. If the width and length of the interconnect is reduced by 30%, then the propagation delay for an interconnect will increase or decrease, by how much %?
2. Reliability issues in CMOS circuits
3. Metal migration in interconnect.
4. Give and explain single phase clock system and explain its drawback.
5. Pipelined system
6. Give & explain carry save adder
7. Short note on Manchester carry circuit.

ASSIGNMENT 2 (DATE : 13th March 2015)

1.	What are the requirements of a clock signal and list the points to be considered in clock distribution.	10
2.	What are the different clocking strategies employed in VLSI systems. Discuss 'H tree' clock distribution in high density CMOS circuits.	
3.	Draw 6T DRAM cell and explain its operation butter-fly plot .	
4.	EEPROM programming technique	
5.	Draw and explain CMOS two-stage OP-AMP.	

6. Switch Capacitor amplifier

BE (ETRX) RAV VIII
8/05/13
Advance VLSI Design

55 : 1st half 13-shilpa(h)

Con. 7493-13. (REVISED COURSE) GS-2965

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data wherever required and justify the **same**.

1. (a) Analog circuits design is difficult as compared to Digital circuit design. Justify. **5**
(b) Explain electromigration effect in an Inter connect. **5**
(c) Draw and explain trench capacitor and stacked capacitor structure of DRAM cell. **5**
(d) Write verilog code for 8-bit counter. **5**

2. (a) Draw the circuit using propagate and generate term for 4-bit CLA network, in **each** of the following :– **10**
(i) nFET logic
(ii) Pseudo nMos logic.

(b) Give and explain the capacitances associated with an interconnect and explain how propagation of signal depends upon the distributed RC effect. **10**

3. (a) The storage capacitor in a DRAM has a value of C_S = 55 fF. The circuitary restricts the capacitor voltage to a value of V_{max} = 3·5 V; When the access transistor is off, the leakage current of the cell is estimated to be 75 nA. **10**
(i) How many electrons can be stored on C_S ?
(ii) How many fundamental charge unit q leave the cell in 1 second due to leakage current ?
(b) Give various important parameter affecting switching performance of C MOS Inverter. Suggest methods to improve it. **10**

4. (a) Give and explain maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. **10**
(b) Implement following functions using AND-OR PLA :– **10**

$X = ac + \bar{b}c$
$Y = abc + \bar{a}\bar{b}c$
$Z = \bar{a}b + ab$

[TURN OVER

56 : 1st half.13-shilpa(h)

Con. 7493-GS–2965-13. 2

5. (a) Give and explain Interconnect scaling with its width, length, thickness and capacitances. **10**

   (b) Give and explain single phase clock system and explain its drowback. **10**

6. (a) Draw and explain C MOS two stage OP-AMP. Give gain boosting technique. **10**

   (b) Draw and explain Schmitt - trigger circuit as a input protection for C MOS. Also explain bi-directional I/O circuits. **10**

7. Write short notes on (any **three**) :– **20**

   (a) Frequency compensation scheme of CMOS Amplifier

   (b) Manchaster carry chain circuits and MODL Circuit

   (c) Pipelined system

   (d) EEP ROM Programming technique.

49 : 2nd half-12-(h) JP

Con. 9126-12. (REVISED COURSE) KR–4398

(3 Hours) [Total Marks : 100

N.B.: (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions from remaining **six** questions.
(3) Draw neat **diagrams** and assume suitable data if **required**.

1. (a) What do you mean by clock skew and clock jitter. 5
   (b) State the need of input and output circuit with their neat diagrams. 5
   (c) What are PVT variations and how does PVT affect integrated circuit. 5
   (d) Analog circuit design is difficult as compared to digital circuit design. Justify. 5

2. (a) What is Elmore delay model. What is the effect of interconnect parasitics on delay ? How delay can be reduced ? 10
   (b) Discuss to concept of charge sharing and explain how it affects reliability of integrated circuit. 10

3. (a) Give and explain to single phase clock system and explain its drawback. 10
   (b) Discuss dynamic CMOS logic. Compare it with static CMOS logic. What is to primary drawback of dynamic CMOS logic. Show to modifications in dynamic CMOS logic to overcome its drawback. 10

4. (a) Show to implementation of four bit carry look ahead adder along with all to equations. 10
   (b) Draw and explain Manchester carry out circuit using carry kill bit. Also draw k-input dynamic Manchester carry chain circuits. 10

5. (a) Draw schematic for 6T SRAM cell and explain its stability criteria. Also draw and discuss its butterfly curve. 10
   (b) Discuss in programming techniques of EEPROM in detail. 10

6. (a) Draw and explain clock generation and stabilization network. Also explain how this clock is distributed in integrated circuit. 10
   (b) Draw and explain MOS based two stage amplifier. Also discuss how frequency compensation can be achieved. 10

7. Write short notes on any **four** :— 20
   (a) DRAM and refresh logic
   (b) Switch capacitor circuit
   (c) Cross talk in integrated circuits
   (d) Interconnect scaling
   (e) Metal migration in interconnect.

(Library) B.E. (Etrx) Sem-VIII (Rev. 5/6/07.

Elective II: VLSI Design.

P4/RT-Ex-07-21

Con. 2931-07. [REVISED COURSE] ND–1801

(3 Hours) [Total Marks : 100

N.B: 1) Question **No.1** is **compulsory**
2) Attempt any **four** out of remaining six questions
3) Assume suitable data wherever **necessary**

1.(a) Explain the switching characteristics of CMOS gate. Suggest the methods to improve the switching performance. [10]

(b) Design one bit full adder using AND, OR, EXOR gates. Write the verilog description of the circuit. Write the stimulus for the full adder [10]

2.(a) Discuss in detail 4 x 4 array multiplier. Can this be used as a building block to create an 8 x 8 multiplier ? If so detail the problems and modifications that need to be made. [10]

(b) Explain EEPROM using floating gate NMOSFETS. [10]

3.(a) Construct a circuit diagram for a CMOS logic gate that implements the AOI function F = A [B + C (D+E)] Design the W/L ratio for the transistors [10]

(b) Design CMOS implementation of JK flip flop .Explain what are the limitations of your design. [10]

4.(a) Summarize the approach you would take to reduce the power dissipation of a CMOS chip that is designed for palm top computer. [10]

(b) What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100pF of on-chip load to satisfy the metal migration consideration (J_{AL} = 0.5 mA/μ)? What is the ground bounce with the chosen Conductor size. The module is 500μm from both the power and the ground Pads and the supply voltage is 5 volts. The rise/fall time of the clock is 1 nsec.(Assume R_s = .05Ω/sq) [10]

5.(a) Discuss floor planning and routing in VLSI. [10]

(b) What is cross talk in integrated circuits? Discuss various methods to reduce it. [10]

6.(a) Explain three main approaches to Design for Testability in detail [10]

(b) Explain in detail Pipelined system design [10]

7 Write short notes on any three :- [20]

a. Behavioral and RTL modeling
b. Resistance and Capacitance Estimation
c. Clock generation and Distribution
d. Carry Look ahead adders

A. VLSI Design

SA list no. 131

Con. 3636-12. (REVISED COURSE) GN-7436

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any four out of remaining six questions.
(3) Assume any suitable data whenever required and justify the same.

1. a) Explain metal migration in interconnect. 5
b) Explain programming techniques of EEPROM using hot electron and Fowler-Northeim emission. 5
c) If the width and length of the interconnect is reduced by 30%, then the propagation delay of an interconnect will increase or decrease, by how much %? 5
d) Draw and explain manchester carry out circuit using carry kill bit. Also draw 4-input dynamic Manchester carry chain circuits. 5

2. a) What would be the conductor width of power and ground wires to a50 MHz clock buffer that drives 100 pF of on-chip load to satisfy the metal-migration consideration ($J_{AL} \approx 0.5mA/\mu m$)? What is the ground bounce with chosen conductor size? The module is 500 µm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1ns. (Assume sheet resistance of wire = 0.05Ω/sq). 10
b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. 10

3. a) Give and explain the drawback with ripple carry adder. Explain 4-bit CLA adder with its carry equations, logical network and write its Verilog description. 10
b) Explain how ESD (electro-static discharge) affect the MOSFET. Give and explain input protection circuits. 10

4. a) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10
b) Draw 4 X 4 pseudo-nMOS ROM array circuitry having stored following data. 0011, 1010, 1100, 0101. Also list the no. of address pins, data pins and word lines. 10

5. a) Explain the need of frequency compensation in CMOS operational amplifier. 10
b) Give and explain single phase clock system and explain its drawback. 10

6. a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. 10
b) What is cross talk in IC's? Explain various methods to reduce it. 10

7. Write short notes on (any three): 20
a) Low power design consideration.
b) Reliability issues in CMOS circuits.
c) Carry save adder.
d) Switch capacitor amplifier.

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Elective II : VLSI Design.

Con. 3006-09. **VR-4179**

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N.B : (1) Question No.**1** is **Compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume **suitable data** wherever **necessary**.

1. (a) Explain various sources of power dissipation in digital CMOS circuits and explain the methods to reduce power dissipation. **10**
   (b) Discuss in detail 4 x 4 array multiplier. Can this be used as a building block to create an 8 x 8 multiplier ? If so detail the problems and modifications that need to be made. **10**

2. (a) Explain the different types of physical fault that can occur in a CMOS chip and relate them to a typical circuit failure. **10**
   (b) Explain EEPROM using floating gate NMOSFETS. **10**

3. (a) Summarize the approach you would take to reduce the power dissipation of a CMOS chip that is designed for palm top computer. **10**
   (b) What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100pF of on-chip load to satisfy the metal migration consideration (J_{AL} = 0.5 mA/μ)? What is the ground bounce with the chosen Conductor size. The module is 500 μm from both the power and the ground Pads and the supply voltage is 5 volts. The rise/fall time of the clock is 1 nsec.(Assume R_s = ·05 Ω/sq). **10**

4. (a) Construct a circuit diagram for a CMOS logic gate that implements the AOI function F = A [B + C (D + E)] Design the W/L ratio for the transistors. **10**
   (b) Design CMOS implementation of JK flip flop. Explain what are the limitations of your design. **10**

5. (a) Discuss floor planning and routing in VLSI. **10**
   (b) Explain in detail Pipelined system design. **10**

6. (a) Explain three main approaches to Design for Testability in detail. **10**
   (b) What is cross talk in integrated circuits ? Discuss various methods to reduce it. **10**

7. Write short notes on any **three** :— **20**
   (a) Behavioral and RTL modeling
   (b) Low power design considerations
   (c) Clock generation and Distribution
   (d) Carry Look ahead adders.

S

PVPP'S

College Of Engineering

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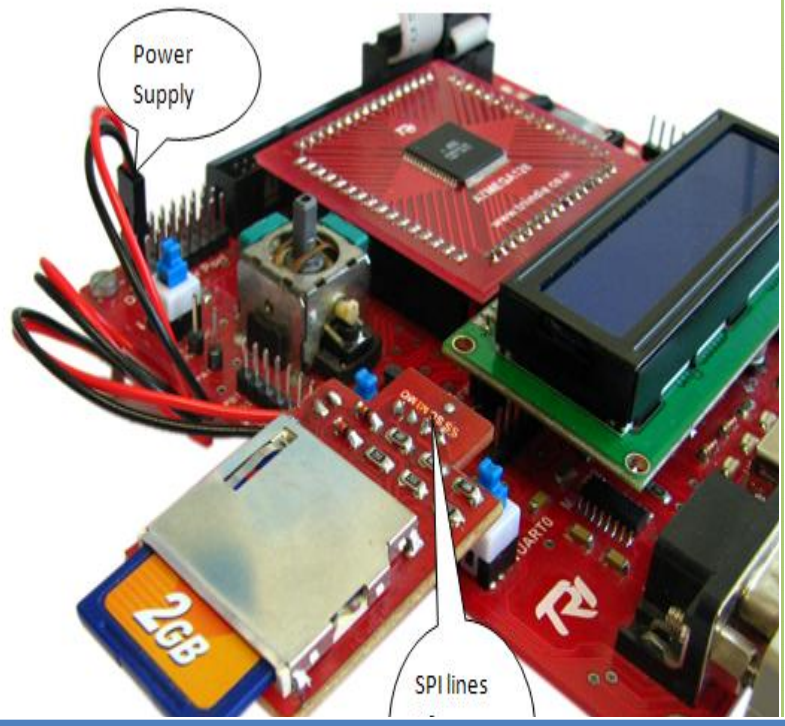


FH 2015

EMBEDDED SYSTEMS AND REAL TIME PROGRAMMING

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
COLLEGE OF ENGINEERING
SINCERITY
SACRIFICE
SYSTEM
1990
Empower The Knowledge

Mrs.ANAGHA DHAVALIKAR

Subject Plan

GROUP NAME : Microprocessors and Microcontrollers	
COURSE TITLE : Embedded Systems and Real-Time Programming **COURSE CODE : B.E. Elex** **SEM : VIII**	
PRE-REQUISITE :DSD-I, DSD-II, MPMC-I, MPMC-II.	

RATIONALE

The aim of the subject is to introduce the students to the concept of Embedded Systems and their application areas. Knowledge of embedded processors like ARM, MSP 430, helps the students to use them while designing an application specific system. It also helps the

OBJECTIVES :

- Learn embedded software architecture and development techniques.
- Understand software and hardware trade-offs that affect embedded system functionality, performance and cost.
- Gain working knowledge of embedded software development process.
- Apply concepts introduced in class to implement a project that utilizes embedded design methodologies and development tools.
- Learn Real-Time hardware and software architecture and development techniques.
- Understand software and hardware trade-offs that affect Real-Time System functionality and performance.
- Gain working knowledge to develop Real-Time Systems.

OUTCOME :

- Knowledge and understanding of fundamental embedded systems design paradigms, architectures, possibilities and challenges, both with respect to software and hardware.
- A wide competence from different areas of technology, especially from computer engineering, robotics, electronics, intelligent systems and mechatronics.
- Deep state-of-the-art theoretical knowledge in the areas of real-time systems, artificial intelligence, learning systems, sensor and measuring systems, and their interdisciplinary nature needed for integrated hardware/software development of embedded systems.

•Ability to analyze a system both as whole and in the included parts, to understand how these parts interact in the functionality and properties of the system, and
•Understanding industrial embedded systems and intelligent embedded system development.

LEARNING RESOURCES: -

Recommended Books:

Sr.No.	Title	Authors	Publisher
T1	Embedded Systems -Architecture, Programming and Design	Rajkamal	Tata McGraw Hill
T2	Embedded Real Time Systems Programming RTOS	Sriram Iyer, Pankaj Gupta	Tata McGraw Hill
T3	Embedded Real Time Systems	K.V.K.Prasad	Dreamtech press
T4	ARM System Developer's Guide	Andrew N.SLOSS, Dominic SYMES	ELSEVIER
R1	Real-Time Concepts for Embedded Systems,	Quing Li, Caroline Yao	Cmpbooks Press
R2	Embedded System Design	Frank Vahid, Tony Givargis	Wiley Publishers
R3	The 8051 Microcontroller and Embedded Systems using assembly and C	Muhammad Ali Mazidi, Janice Gillispie Mazidi	Pearson Education
R4	Embedded Sytems Architecture	Tomy Noergard	ELSEVIER
R5	An Embedded Software Primer RTOS	David E.Simon	Pearson Education
R6	Texas Manual	Texas Instruments	
R7	Fundamentals Of Embedded Software	Daniel Lewis	Prentice Hall

COURSE MATERIALS MADE AVAILABLE

- Course instructional objectives & outcomes
- Syllabus
- Chapte rwise Question Bank

Evaluation :

	Hours	Marks
Theory Examination	3	100
Practical Examination	–	–
Oral Examination	–	25
Term work	–	25
Total		150

The students will be evaluated on the basis of four tests (2 written tests, 1 oral and 1 on line test) conducted during the semester

List of Experiments

Suggested Laboratory Experiments:
Minimum six experiments covering the topics in syllabus

- Interfacing keyboard, LED, LCD displays.
- Serial Communication.
- Programming should be done using a suitable IDE and Embedded C.

Expt. No.	Name of the Experiments
1	Learning Concepts in ARM7 Microprocessor.
2	Interface LED with LPC 2148
3	Interface Seven Segment Dispplay with LPC 2148
4	Interface LCD Display with LPC 2148
5	Interface a Hex Keypad with LPC 2148
6	Serial Communication with LPC 2148
7	Interface a Buzzer with LPC 2148

Chapter wise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 1

Chapter Name : Introduction to Embedded systems

Approximate Time Needed : 4hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction to Embedded system.
2	Design Metrics, Hardware &software co-design.
3	Embedded memories &sensors.
4	Embedded cores.

Objectives: To teach students :-
- Different core in embedded system
- Types of embedded memories.

Outcomes: students will learn:-
- What do we mean by embedded systems.
- Various embedded cores and memories

Model Questions:

No.	Questions	Year	Marks
1	Differentiate between RISC and CISC Processors.	May-2011	6
		Dec-2012	5
2	Explain different types of Embedded memories.	May-2011 Dec-2011	5
3	What is H/W and S/W co-design?	May-2012	5
4	Explain System on Chip (SOC).	May-2012	5
5	Explain with suitable example the following challenges met by an Embedded System Designer: I) Execution Performance II) Power Consumption III) Time to Market IV) Memory space V) Debugability VI) Cost	Dec-2012	12
6	Explain classification of Embedded system with suitable examples.	Dec-2012	8
7	Discuss design metric issues faced while designing an embedded system with the help of an example.	May-2013	5
8	Discuss and compare various embedded micro controller cores like RISC, CISC, SOC, ARM.	May-2013	5
10	Differentiate between RISC and CISC processor.	Dec-2013	5
11	What is H/W and S/W co-design?	Dec-2013	5
12	Discuss design metric issues in designing an embedded system. Give suitable example.	May-2014	5
13	Explain operating modes of ARM7TDMI.	May-2014	5

Chapterwise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 2

Chapter Name : Introduction to MSP 430 RISC Controllers

Approximate Time Needed : 12hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
5	Introduction to MSP430.
6	Types of MSP 430. Need of MSP430.
7	Addressing mode of MSP 430.
8	Low power mode of MSP430.
9	Introduction to ARM.
10	Types of addressing modes in ARM.
11	Instruction set of ARM.
12	Interrupts &exceptions in ARM.
13	Floating &fixed point conversions.
14	DSP features of ARM.
15	Digital signal controllers.
16	DSC difference with conventional Micro controllers

Objectives:To teach student:-
- Need of MSP 430.
- Addressing modes of MSP 430.
- Addressing modes of ARM.
- Instructions in MSP 430
- Instructions in ARM.

Outcomes: students will learn:-
- How to write ASP (Assembly Language Program).
- How to choose MSP depending upon application.

Model Questions

No.	Questions	Year	Marks
1	Explain various operating modes of ARM/ARM7 processors.	May-2011	10
		Dec-2011	10
		Dec-2012	10
2	Explain the register set of MSP-430 RISC controller (working registers, SFRs, Status registers etc.)	May-2011	10
		Dec-2012	10
3	Write a detailed note on THUMB mode of operation of ARM processor.	May-2011	10
4	Write a note on Digital Signal Controllers.	May-2011	5
		Dec-2011	5
		Dec-2012	5

5	Briefly explain Exceptions of ARM7	Dec-2011	10
6	Explain address space (Memory map) of MSP – 430.	Dec-2011	10
7	Explain basic clock model of MSP-430.	Dec-2011 May-2012	10 10
8	Explain functions of different registers available in ARM7.	May-2012	5
9	Draw and explain status register structure of MSP 430.	May-2012	5
10	Explain different Exceptions which occur in MSP - 430	May-2012	5
11	Explain Processor modes of ARM7, also specify different branch instruction used to exchange branch from ARM mode to THUMB mode.	May-2012	10
12	Explain different addressing modes of ARM7TDMI.	May-2012	10
13	Draw MSP 430 architecture and write its specifications.	Dec-2012	5
14	Explain why ARM processor is one of the most commonly used 32 bit embedded processor. Draw architecture of ARM7 TDMI processor.	Dec-2012	10
15	Describe addressing modes of MSP 430 or ARM7TDMI.	May-2013	5
16	Describe the operating modes and basic clock modules of MSP 430.	May-2013	10
17	Provide description of exceptions in ARM7TDMI (interrupts).	May-2013	10
18	Explain THUMB mode ofARM7TDMI core and compare it with normal mode.	May-2013	10
19	Explain status register of MSP 430.	Dec-2013	5
20	Explain operating modes of ARM 7 and also explain Registers available in each mode.	Dec-2013	10
21	Explain clock circuit and registers used to control function of clock module of MSP 430.	Dec-2013	10
22	Compare and explain ARM7 with ARM7TDMI.	Dec-2013	10
23	Explain Interrupt Latency with example and what are the factors responsible for Interrupt Latency?	Dec-2013	5
24	Explain SPI protocol for serial communication.	May-2014	5
25	Explain clock circuit and registers used to control function of clock module of MSP 430.	May-2014	10
26	Stock implementation in ARM7. --2	May-2014	5

Chapterwise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 3

Chapter Name : Serial communications

Approximate Time Needed : 8hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
17	Introduction to SCI.
18	Introduction to SPI.
19	Various C ISR Declaration syntaxes
20	Interrupt Vectors, Priorities and Nesting
21	Tick Timer Interrupt as heart-beat of embedded system
22	7-Seg LED, Segment-LCD, Alphanumeric LCD, Graphic LCD displays
23	Introduction to RS 485 and Modbus protocol, Ethernet and TCPIP Stack
24	CAN features and protocols

Objectives:To teach students:-
- Types serial communication.
- CAN protocol in detail.
- Interfacing of different peripheral.

Outcomes: student will learn:-
- Interfacing different devices with ARM.
- Interrupt structures, priorities &exceptions.

Model Questions

No.	Questions	Year	Marks
1	Explain the interface of Alphanumeric LCD with any micro controller of your choice. (Draw neat diagram).	May-2011	7
2	Write a detailed note on the CAN Bus explaining its features and protocols.	May-2011 Dec-2012	7 5
3	What is interrupt latency in Embedded systems? Suggest methods to reduce latency.	May-2011	10
4	Write a note on Watchdog timer.	May-2011	5
5	Write a note on Serial Peripheral Interface (SPI)	May-2011 Dec-2011 Dec-2012	5 5 5
6	Write short note on : Difference between RS232 and RS 485	Dec-2011 Dec-2012	5 5
7	Draw and explain data frame format of CAN bus.	May-2012	5
8	Write short note on: SPI and SCI port.	May-2012	5

9	Explain various basic serial communication methods.	May-2013	5
10	With the help of suitable block diagram explain: i) Graphic LCD ii) RS 232/485 iii) PWM DC motor (speed control) interfacing	May-2013	10
11	Give need for interprocess communication and synchronization. Describe the methods of the same (IPC) in detail.	May-2013	10
12	Give features of CAN and explain protocol.	May-2013	5
13	Draw and explain CAN bus frame format.	Dec-2013	5
14	Describe with suitable diagram, SPI interface.	Dec-2013	5
15	Discuss layered architecture of CAN node. Elaborate Transfer layer with regards to massage framing and arbitration.	May-2014	10
16	with the help of suitable diagram explain: i) LCD interface ii) Hex keypad interface.	May-2014	10
17	Techniques used in Interprocess Communication in Embedded System.	May-2014	5

Chapterwise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 4

Chapter Name : Software Programming in Assembly Language (ALP) and in High Level Language 'C'

Approximate Time Needed : 08hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
25	Need of C language based programming.
26	Advantages &disadvantages of C programming.
27	'C' program elements: Macros &Functions.
28	Data types, Data structure, Modifiers.
29	Statements, Loops and pointers.
30	Queues, Stacks, Lists in C.
31	Compilers and Cross compilers in C.
32	Source Code Engineering Tools for Embedded C/C++, Optimization of Memory Needs

Objectives:To teach students:-
- Data types, element &data structures in C.
- Compiler &cross compiler in C.

Outcomes: student will learn:-
- How to write a program in embedded C.

Model Questions

No.	Questions	Year	Marks
1	Differentiate between Object Oriented and Procedure language	Dec-2011	5
2	Explain Data Structures, Queue, Circular Queue, Linked List, Array.	May-2012	10
3	Compare software programming in in assembly and C programming language.	May-2013	5
	With the help of suitable examples, describe following C-program elements i) Header File ii) Preprocessor Directives iii) Macro functions iv) Modifiers v) Link-List	May-2013	10
4	Describe embedded programming tools like compiler, cross complier, integrated development environment, debugging tools in circuit emulator	May-2013	5
5	Differentiate between procedure and object oriented language.	Dec-2013	5

6	Explain Data Structure Queue, Circular Queue, Link list and Array with respect to Embedded C Programming.	Dec-2013	10
7	Justify use of C programming for embedded software development.	May-2014	5
8	Explain data structure queue, circular queue, Link list and array in embedded system.	May-2014	10
9	Write ARM assembly language program to implement $\sum_{i=1}^{N} fXI for i = 1 to N$	May-2014	10
10	Describe embedded programming tools like compiler, cross complier, integrated development environment, in circuit emulator.	May-2014	10

Chapterwise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 5

Chapter Name : Real-time concepts

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
33	Introduction to RTOS
34	Characteristic of RTOS.
35	Real world issues
36	Concepts of task, threads, process.
37	Multitasking.
38	Task scheduling.
39	Device drivers.
40	Inter task communication
41	How to choose RTOS.
42	Overview of RTOS.

Objectives:To teach students:-
- Characteristics of RTOS.
- Different concepts of RTOS.
- How to choose RTOS.

Outcomes: student will learn:-
- Characteristics of RTOS
- Different concepts of RTOS

Model Questions

No.	Questions	Year	Marks
1	Suggest various techniques used for interprocess communication in an embedded system with relevant examples. Also explain strategies used for synchronization between processes.	May-2011	15
2	With the help of a neat diagram, explain the different states a task can be in and the transitions between them.	May-2011	5
3	What is the shared data problem? Explain various techniques to overcome it. (with relevant examples)	May-2011 May-2012	10 10
4	Explain bounded and unbounded priority inversion problem. Suggest methods to overcome/minimize it.	May-2012	10
5	Explain task and task states.	Dec-2011	5
6	What is bounded and unbounded priority inversion problem? Explain with a suitable example what is Priority Inheritance Protocol.	Dec-2012	10
7	Discuss various types of Semaphore in detail.	Dec-2011	10
8	A real time program has three tasks with the following	Dec-2011	10

	characteristics: Determine whether the program will meet its deadline if scheduled according to priorities and with pre-emption.		

	Priority	Period	CPU time
T1	1	6	2
T2	2	18	14
T3	3	36	6

9	Explain in detail Mutex, Pipes, Queues and Mailboxes.	Dec-2011	10
10	Write short note on: Interprocess communication.	Dec-2011 Dec-2012	5 5
11	Differentiate between Mutex, Lock () and Spinlock () interprocesss communication techniques with suitable example.	May-2012	5
12	Name different problems of using Semaphore also explain priority inversion problem and its solution.	May-2012	10
13	Define Process, threads and Tasks. Also explain various status of task.	May-2012	10
14	Three tasks with ids T1, T2, T3 with estimated time 10,5,7 ms and priority 1,3,2 respectively enters the ready queue together. A new process T4 with estimated time 2 ms and priority 0 enters the ready queue after 2 ms. Schedule the tasks using preemptive SJF(shortest job first) and priority based Scheduling algorithm. Calculate execution time, waiting time, turnaround time, mention which is the best scheduling algorithm for a given problem. (0 is the highest priority)	May-2012	10
15	Write short note on: Periodic and Aperiodic Rate Monotonic Scheduling.	May-2012	5
16	Compare schedulers used in hard real time systems.	Dec-2012	10
17	An embedded system with task ids T1, T2, T3 with estimated completion time 12,6,8 ms and priorities 1,3,2 respectively moves to ready queue together. A new process T4 with estimated time 5 ms and priority 0 enters the ready queue after 4 ms of start of execution of T1. Assume all the tasks contain only CPU operation. Calculate the waiting time and turnaround time for each task and the average waiting time and turn around time using priority based pre-emptive algorithm. (0 is the highest priority)	Dec-2012	10
18	What is shared data problem? Explain different types of semaphores.	Dec-2012	10
19	Write short notes on: Different states of tasks.	Dec-2012	5
20	For the given task calculate:	May-2013	10

<table>
<tr><td></td><td>i) waiting time
ii) turnaround time
for Shortest Job First (SJF) and Earliest Deadline First (EDF) scheduling. Comment on the result. All tasks entered ready queue at same time.
<table>
<tr><td>Task ID</td><td>Execution Time</td><td>Deadline</td></tr>
<tr><td>T1</td><td>06</td><td>39</td></tr>
<tr><td>T2</td><td>16</td><td>30</td></tr>
<tr><td>T3</td><td>18</td><td>45</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>21</td><td>What is real time system? Compare RTOS with traditional OS. Discuss interrupts with respect to real time behavior.</td><td>May-2013</td><td>10</td></tr>
<tr><td>22</td><td>Explain priority inversion problems and solutions.</td><td>May-2013</td><td>5</td></tr>
<tr><td>23</td><td>Suggest various techniques used for interprocess communication in an embedded system.</td><td>Dec-2013</td><td>10</td></tr>
<tr><td>24</td><td>What is bounded and unbounded priority inversion ? Also explain how it is solved using priority inheritance and priority ceiling.</td><td>Dec-2013</td><td>10</td></tr>
<tr><td>25</td><td>Explain different pre-emptive scheduling policies with suitable examples.</td><td>Dec-2013</td><td>10</td></tr>
<tr><td>26</td><td>What is bounded and unbounded priority inversion problem? Suggest solutions used for the same. Explain with suitable example.</td><td>May-2014</td><td>10</td></tr>
<tr><td>27</td><td>For the given task table calculate:
i) waiting time
ii) turn around time
for earlist deadline first scheduling (EDF). All tasks entered ready queue at the same time.
<table>
<tr><td>Task ID</td><td>Execution Time</td><td>Deadline</td></tr>
<tr><td>T1</td><td>06</td><td>39</td></tr>
<tr><td>T2</td><td>16</td><td>30</td></tr>
<tr><td>T3</td><td>18</td><td>45</td></tr>
</table></td><td>May-2014</td><td>10</td></tr>
<tr><td>28</td><td>What is shared data problem? Explain various techniques to overcome shared data problem.</td><td>May-2014</td><td>10</td></tr>
</table>

Chapterwise Plan

Subject Title: Embedded Systems &Real Time Programming

Chapter No. : 6

Chapter Name : Fundamentals of Design and Development

Approximate Time Needed : 06hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
43	Program modeling tools. Testing and debugging technologies.
44	Application of embedded system in various FIELD.
45	Case study of home automation.
46	Case study of medical automation
47	Case study of industrial automation
48	Case study of robotics automation

Objectives: To teach students:-

- Different applications of RTOS.
- Applications of Embedded Systems.

Outcomes: Students will learn:-

- to design different RTOS based systems.
- to uderstand the different application areas of embedded systems.

Model Question

No.	Questions	Year	Marks
1	Explain what is the Linear sequential model in Embedded software development.	May-2011	10
2	Explain the various program modeling techniques used in embedded system design.	May-2011	10
3	Design a FSM (Finite State Machine) for a simple elevator control system. The building has three total floors (G+2). Each floor has a call button and there are three buttons inside the elevator to choose the desired floor, discuss the operation of the system through the FSM.	Dec-2011	10
4	Explain waterfall model of embedded software development.	Dec-2011	10
5	Write short notes on: a) Programming models b) Spiral model used in EDLC c) Black box and white box testing	 Dec-2011 May-2012 Dec-2011 May-2012	 5 5 5 5
6	Design an automatic Tea and Coffee vending machine based on	May-2012	7

	FSM (Finite State Machine) Model for the following requirement the tea/coffee vending is initiated by the user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.		
7	Draw and explain Petrinet model.	May-2012	3
8	List and explain hardware and software tools of an embedded system.	Dec-2012	10
9	Explain various programming modelling techniques used in Embedded system design.	Dec-2012	10
10	Design a car control embedded system with following specifications/features: i) It is an electric car. ii) Steering angle, acceleration, direction (R/F) are inputs from driver. Iii) It control speed, left/right steering, forward/backward direction iv) Displays speed For designing above system give 1) Show block diagram for hardware 2) Software modules/drivers diagram, flowchart 3) FSM/Petrinet model of the system. 4) Real time challenges and solutions. 5) Suggest hardware and software solutions/tools used. 6) Suggest testing, debugging, realtime issues.	May-2013	20
11	For an embedded system, prepaid electricity meter , whose units (readings) are down loaded wirelessly. Also a parallel LCD of a meter is installed in the house. Discuss the necessary hardware required with justification. Support your answer with suitable block diagram of the embedded electricity meter.	Dec-2013	12
12	Design an automatic tea and coffee vending machine based on FSM model for the following requirement. The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.	Dec-2013	8
13	Explain spiral model used in EDLC. Note on: Black Box and White Box Testing	Dec-2013	5 5
14	Design an embedded system to measure frequency of a power line. Suggest hardware components used. Also give software architecture for the system.	May-2014	10
15	Note on: Petrinet modelling	May-2014	5
16	Note on: Waterfall model in embedded Software Development	May-2014	5

Assignment – 1 (Date:- 9th Feb. 2015)

- Explain various operating modes of ARM/ARM7 processors.
- Differentiate between RISC and CISC Processors.
- Explain different types of Embedded memories.
- Explain operating modes of ARM7TDMI.

- Explain the register set of MSP-430 RISC controller (working registers, SFRs, Status registers etc.)
- Explain basic clock model of MSP-430.
- Write a note on Serial Peripheral Interface (SPI)
- Write a detailed note on the CAN Bus explaining its features and protocols.

Assignment – 2 (Date:- 13th March 2015)

- What is the shared data problem? Explain various techniques to overcome it. (with relevant examples)
- Three tasks with ids T1, T2, T3 with estimated time 10,5,7 ms and priority 1,3,2 respectively enters the ready queue together. A new process T4 with estimated time 2 ms and priority 0 enters the ready queue after 2 ms. Schedule the tasks using preemptive SJF(shortest job first) and priority based Scheduling algorithm. Calculate execution time, waiting time, turnaround time, mention which is the best scheduling algorithm for a given problem. (0 is the highest priority)
- Describe embedded programming tools like compiler, cross complier, integrated development environment, debugging tools in circuit emulator
- Differentiate between procedure and object oriented language.
- Describe embedded programming tools like compiler, cross complier, integrated development environment, debugging tools in circuit emulator Differentiate between procedure and object oriented language.
- Design a FSM (Finite State Machine) for a simple elevator control system. The building has three total floors (G+2). Each floor has a call button and there are three buttons inside the elevator to choose the desired floor, discuss the operation of the system through the FSM.
- Write short notes on:
  a) Programming models
  b) Spiral model used in EDLC
  c) Black box and white box testing
- Design an automatic tea and coffee vending machine based on FSM model for the following requirement. The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin.

Question Papers

May – 2014

Question no. 1 is compulsory
Attempt any 4 out of remaining questions

Q.1

- Discuss design metric issues in designing an embedded system. Give suitable example. 5
- Explain SPI protocol for serial communication. 5
- Explain operating modes of ARM7TDMI.1 5
- Justify use of C programming for embedded software development. 5

Q. 2

- Explain data structure queue, circular queue, Link list and array in embedded system. 10
- Explain clock circuit and registers used to control function of clock module of MSP 430. 10

Q.3

- Design an embedded system to measure frequency of a power line. Suggest hardware components used. Also give software architecture for the system. 10
- Write ARM assembly language program to implement 10

$$\sum_{i=1}^{N} f(X_i) \text{ for } i = 1 \text{ to } N$$

Q. 4

- Discuss layered architecture of CAN node. Elaborate Transfer layer with regards to massage framing and arbitration. 10
- with the help of suitable diagram explain: 10
  i) LCD interface
  ii) Hex keypad interface.

Q.5

- What is bounded and unbounded priority inversion problem? Suggest solutions used for the same. Explain with suitable example. 10
- For the given task table calculate:

i) waiting time
ii) turn around time
for earliest deadline first scheduling (EDF). All tasks entered ready queue at the same time.

Task ID	Execution Time	Deadline
T1	06	39
T2	16	30
T3	18	45

Q. 6

- Describe embedded programming tools like compiler, cross complier, integrated development environment, debugging tools in circuit emulator. 10
- What is shared data problem? Explain various techniques to overcome shared data problem. 10

Q.7 Write short notes on (Any three) 20

- Petrinet modelling
- Waterfall model in embedded Software Development
- Stock implementation in ARM7.
- Techniques used in Interprocess Communication in Embedded System.

Dec – 2013

Question no. 1 is compulsory
Attempt any 4 out of 6 questions

Q.1

- Differentiate between RISC and CISC processor. 5
- Draw and explain CAN bus frame format. 5
- Explain status register of MSP 430. 5
- Differentiate between procedure and object oriented language. 5

Q.2

- Explain operating modes of ARM 7 and also explain Registers available in each mode. 10
- Explain clock circuit and registers used to control function of clock module of MSP 430. 10

Q. 3

- Compare and explain ARM7 with ARM7TDMI. 10
- Describe with suitable diagram, SPI interface. 5
- Explain Interrupt Latency with example and what are the factors responsible for Interrupt Latency? 5

Q.4

- Suggest various techniques used for interprocess communication in an embedded system. 10
- Explain Data Structure Queue, Circular Queue, Link list and Array with respect to Embedded C Programming. 10

Q. 5

- What is bounded and unbounded priority inversion ? Also explain how it is solved using priority inheritance and priority ceiling. 10
- Explain different pre-emptive scheduling policies with suitable examples. 10

Q. 6

- For an embedded system, prepaid electricity meter , whose units (readings) are down loaded wirelessly. Also a parallel LCD of a meter is installed in the house. Discuss the necessary hardware required with justification. Support your answer with suitable block diagram of the embedded electricity meter. 12

•Design an automatic tea and coffee vending machine based on FSM model for the following requirement. The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin. 8

Q. 7

Write a short note on: 20

1. Explain spiral model used in EDLC.
2. What is H/W and S/W co-design?
3. Black Box and White Box Testing.

May – 2013

Question no. 1 is compulsory

Attempt any 4 out of 6 questions

Q.1

•Discuss design metric issues faced while designing an embedded system with the help of an example. 5

•Describe addressing modes of MSP 430 or ARM7TDMI. 5

•Explain various basic serial communication methods. 5

•Compare software programming in assembly and C programming language. 5

Q. 2

•Describe the operating modes and basic clock modules of MSP 430. 10

•Provide description of exceptions in ARM7TDMI (interrupts). 10

Q. 3

•Explain THUMB mode ofARM7TDMI core and compare it with normal mode. 10

•With the help of suitable block diagram explain: 10

i) Graphic LCD
ii) RS 232/485
iii) PWM DC motor (speed control) interfacing

Q. 4

•With the help of suitable examples, describe following C-program elements- 10

i) Header File
ii) Preprocessor Directives
iii) Macro functions
iv) Modifiers
v) Link-List

•For the given task calculate: 10

i) waiting time
ii) turnaround time for Shortest Job First (SJF) and Earliest Deadline First (EDF) scheduling. Comment on the result. All tasks entered ready queue at same time.

Task ID	Execution Time	Deadline
T1	06	39
T2	16	30
T3	18	45

Q.5

- Give need for interprocess communication and synchronization. Describe the methods of the same (IPC) in detail. 10
- What is realtime system? Compare RTOS with traditional OS. Discuss interrupts with respect to real time behaviour. 10

Q.6

- Design a car control embedded system with following specifications/features: 20

i) It is an electric car.
ii) Steering angle, acceleration, direction (R/F) are inputsfrom driver.
Iii) It control speed, left/right steering, forward/backward direction
iv) Displays speed

For designing above system give

1) Show block diagram for hardware
2) Software modules/drivers diagram, flowchart
3) FSM/Petrinet model of the system.
4) Real time challenges and solutions.
5) Suggest hardware and software solutions/tools used.
6) Suggest testing, debugging, real time issues.

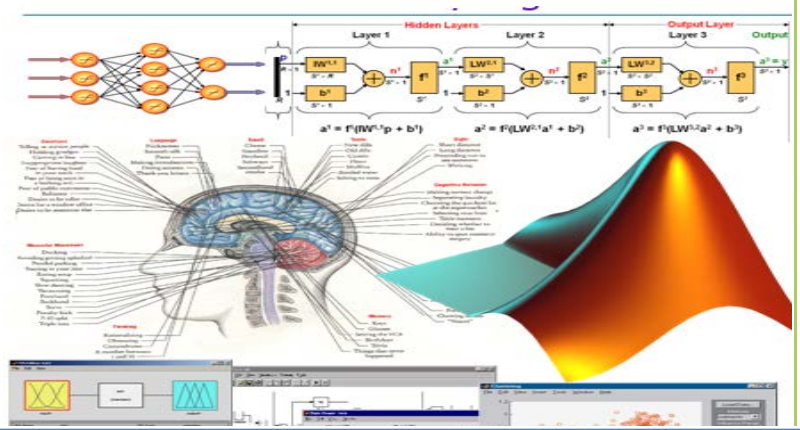
Q. 7 Attempt any three 20

- Discuss and compare various embedded micro controller core like RISC, CISC, SOC, ARM.
- Give features of CAN and explain protocol.
- Describe embedded programming tools like compiler, cross complier, integrated development environment, in circuit emulator.
- Explain priority inversion problems and solutions.

PVPP'S

College Of Engineering

ELEC



FH 2015

NEURAL NETWORK AND FUZZY SYSTEMS

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY
SACRIFICE
SYSTEM
1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mrs.NILIMA ZADE

Subject Plan

GROUP NAME: SIGNALS AND SYSTEM
COURSE TITLE: Neural Network and Fuzzy system **SEM : VIII(FH 2015)**
PRE-REQUISITE: This subject requires the student should have knowledge in the basic techniques of mathematics and computer programming language such as C, C++,Java, Matlab

RATIONALE

This course covers basic concepts of artificial neural networks, fuzzy logic systems and their applications. Its focus will be on the introduction of basic theory, algorithm formulation and ways to apply these techniques to solve real world problems.

OBJECTIVES :

12. To expose the students to the concepts of feed forward neural networks.
13. To provide adequate knowledge about feedback neural networks.
14. To teach about the concept of fuzziness involved in various systems.
15. To provide adequate knowledge about fuzzy set theory.
16. To provide comprehensive knowledge of fuzzy logic control and adaptive fuzzy logic and to design the fuzzy control using genetic algorithm.
17. To provide adequate knowledge of application of fuzzy logic control to real time systems.
18. To emphasize intuitive understanding and practical implementations of the theoretical concepts.
19. To develop an appreciation of the application of his/her knowledge in actual industry and project work.

20. To prepare the students to excel in post graduate studies.

OUTCOME :

On completion of the module, the students should be able to:

1. Knowledge and understanding: Understanding principles of neural networks and fuzzy logic fundamentals; Design the required and related systems.
2. Basics of Neural Networks and essentials of Artificial Neural Networks with Single Layer and Multilayer Feed Forward Networks.
3. Various neural network and fuzzy systems models and the applications of these models to solve engineering problems.
4. Graduates can work as freelance consultants or advisers and carry out research and technological development tasks.
5. Students shall solve complex problems utilizing discipline specific expertise.

LEARNING RESOURCES: -

RECOMMENDED BOOKS:-

- Simon Haykin, *"Neural Network* a - *Comprehensive Foundation",* Pearson Education
- Dr.S.N.Sivanandam,Mrs S.N. Deepa Introduction to Soft computing tool Wiley Publication
- Satish Kumar Neural Networks:A classroom Approach Tata McGraw-Hill
- Zurada J.M., *"Introduction to Artificial Neural Systems,* Jaico publishers
- Thimothv J. Ross, "Fuzz *V Logic with Engineering Applications",* McGraw
- Ahmad Ibrahim, *"Introduction to Applied Fuzzy Electronics',* PHI
- Rajsekaran S, Vijaylakshmi Pai, Neural Networks, Fuzzy Logic, and Genetic Algorithms, PHI

- Hagan, Demuth, Beale, 'Neural Network Design', Thomson Learning
- Christopher M Bishop Neural Networks For Pattern Recognition ,Oxford Publication
- William W Hsieh Machine Learning Methods in the Environmental Sciences Neural Network and Kernels Cambridge Publication
- Dr.S.N.Sivanandam,Dr.S.Sumathi Introduction to Neural Network Using Matlab Tata McGraw-Hill

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapter wise Question Bank

Evaluation :

Theory Exam	100 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Atleast 10 experiments based on the entire syllabus

Expt.No.	Name of the Experiments
1	To design and simulate perceptron learning rule for single layer single discrete perceptron using MATLAB/SCILAB
2	To simulate testing(Recall) perceptron learning rule for single layer single discrete perceptron
3	To design and simulate perceptron learning rule for single layer multiple discrete perceptron using MATLAB/SCILAB
4	To simulate testing(Recall) perceptron learning rule for single layer multiple discrete perceptron
5	To design and simulate delta learning rule for single layer single continuous perceptron using MATLAB/SCILAB
6	To simulate testing(Recall) delta learning rule for single layer single continuous perceptron
7	To design and simulate Back propagation algorithm for multi layer continuous perceptron using MATLAB/SCILAB
8	To design and simulate radial basis function for multi layer continuous perceptron using MATLAB/SCILAB
9	To design and implement different fuzzy membership functions using MATLAB/SCILAB
10	To design and simulate different fuzzy operations (Union , intersection, complement, fuzzy dilation and contraction)using MATLAB/SCILAB
11	To Design and simulate fuzzification process for fuzzy controller of washing machine using MATLAB/SCILAB
12	To Design and simulate Defuzzification process for fuzzy controller of washing machine using MATLAB/SCILAB
13	Application of Fuzzy System (Design fuzzy controller for Train break system)

Chapterwise Plan

Subject Title:Neural Network and Fuzzy system

Chapter No. : 1

Chapter Name : Introduction to Artificial neural network

Approximate Time Needed : 8hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction,Biological neuron
2	McCulloch and Pitts models of neuron, types of activation function.
3	Network architectures
4	Knowledge representation learning process: Error correction learning
5	Supervised unsupervised learning
6	Learning Rules.
7	Learning Rules.
8	Learning Rules.

Objectives:

The Student will learn

1. Basic model of artificial neuron.
2. Different network architecture.

3. Different types of learning and learning Rules.

Lesson Outcome:

After completion of this module student will be able to understand

1. Principle of Artificial neural network,basics of neural network and essentials of neural network.
2. Supervised and unsupervised learning
3. Different learning rules.

Model Questions:

JUNE 2014

1. Explain different network architecture.

DEC 2013

(a) Write perceptron training algorithm for several output cases. **5**
(b) Explain Widrow-Hoff learning rule. **5**

Write short notes on (any **four**) :—
(a) Types of activation functions
(d) What are various characteristics of ANN.

(a) What is learning process ? What do you mean by supervised and unsupervised learning with suitable example ? **10**

Chapterwise Plan

Subject Title: Neural Network and Fuzzy system

Chapter No. : 2

Chapter Name : **Single layer Perceptron**

Approximate Time Needed : 8hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
9	Perceptron learning rule, Algorithm .
10	Discriminate function, classification pattern.
11	Perceptron convergence theorem.
12	Numerical based on above topic.
13	Steepest descent algorithm
14	Least mean square algorithm.
15	Single layer perceptron network and algorithm,SCPTA.
16	Numerical based on above topic

Objectives:

Student will learn single layer perceptron network and its algorithms

Lesson Outcomes:

On completion of this module student will be to implement single layer perceptron learning rules.

Model Questions:

1. Explain linearly separable and nonseparable pattern classification.
2. Explain LMS algorithm
3. Explain Steepest descent algorithm
4. Explain perceptron convergence theorem
5. Perform two training steps (epoch) of the network using delta learning rule for lambda is 1 and learning constant is 0.25. Given data pair is (X1= $[2\ 0\ -1]^T$, $d_1 = -1$), (X_2= $[1\ -2\ -1]^T$, $d_2 = 1$) Initial weights are $W_1 = [1\ 0\ 1]^T$. Use bipolar continuous activation function.

Chapterwise Plan

Subject Title: Neural Network and Fuzzy system
Chapter No. : 3 Chapter Name :**Multi layer Perceptron** Approximate Time Needed : 6hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
17	R caregory perceptron network
18	Need of multilayer, Multilayer feedforword network. MCPTA
19	Back propagation algorithm
20	Back propagation algorithm
21	Learning factors.
22	Learning Factors

Objectives:

Student will learn Multi layer perceptron network and its algorithms

Outcome: On completion of this module student will be to implement Multi layer perceptron training algorithm .

Model Questions:

15. Explain in detail error back propagation training algorithm.

16. Prove f '(net) = y(1- y) if f(net)= y = $\frac{1}{(1+e^{-net})}$

17. What are the learning factors.

Chapterwise Plan

Subject Title: Neural Network and Fuzzy system

Chapter No. : 4

Chapter Name :**Radial Basis and Recurrent Neural Network**

Approximate Time Needed : 08hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
23	RBF network structure and reparability of patterens
24	RBF learning structure strategies
25	K- MEANS Algorithm
26	LMS algorithm
27	Comparision of RBF and MLP networks
28	Hopfield networks: energy function
29	Spurious state
30	Error performance

Objectives:

Objective: Student will learn RBF network and its algorithms

Lesson Outcomes

On completion of this module student will be to implement Radial basis training algorithm.

Model Questions:

1. Compare between RBF and MLP.
2. Write short note on Hopfield network.

3. Explain Spurious state
4. Solve XOR by RBF

Chapterwise Plan

Subject Title: Neural Network and Fuzzy system
Chapter No. : 5 Chapter Name :**Neuro-dynamics** Approximate Time Needed : 08hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
31	Introduction
32	Attractors
33	Neurodynamical model
34	Adaptive Resonance theory
35	SOFM : self organizing feature map
36	SOFM
37	Brain state in a box model
38	Numerical based on above topic

Objectives:

Student will learn self organizing feature map and brain state in a box model and its algorithms

Outcomes:

On completion of this module student will be to understand SOFM and neurodynamicalmodel .

Model Questions:

5. What are the salient features of Kohonen'sself organizing learning algorithm?
6. Explain Boltzmann's learning.\
7. Write short note on

a. Self organizing feature map.
b. Brain state in Box mode

Chapterwise Plan

Subject Title: Neural Network and Fuzzy system
Chapter No. : 6 Chapter Name : **Fuzzy Logic** Approximate Time Needed : 10hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
39	Fuzzy set
40	Fuzzy properties
41	Operation on fuzzy set
42	Fuzzy relation
43	Fuzzy membership functions
44	Fuzzification methods
45	Defuzzification methods
46	Fuzzy controllers: fuzzy controller for traction system
47	fuzzy controller for washing machine
48	fuzzy controller for Domestic shower

Objectives:

Student will learn

1. Fuzzy logic and fuzzy set theory
2. Fuzzification and defuzzification methods
3. Fuzzy logic controllers

Lesson Outcomes:

On completion of this module student will be to implement fuzzy logic controller for washing machine, train or different fuzzy based real time system .

Model Questions:

1. Fuzzy set A $\underset{\sim}{A}$= $\{\frac{0.1}{0}+\frac{0.4}{1}+\frac{1}{2}+\frac{0.3}{3}+\frac{0.2}{4}\}$

Fuzzy set B = $\{\frac{0.2}{0}+\frac{0.5}{1}+\frac{1}{2}+\frac{0.4}{3}+\frac{0.1}{4}\}$

Find the following i] A∪ B, ii] A∪ B),iii](A)$_{0.4}$, iv] $\overline{A}$ ∪ B,

v] $\overline{\text{A ∪ B}}$

2. Fuzzy set X = {(0.2,x_1),(0.5,x_2),(0.8,x_3),(1.0,x_4),(0.6,x_5),(0.1,x_6)}

Fuzzy set Y = {(0.3,y_1),(0.6,y_2),(0.9,y_3),(1.0,y_4),(0.6,y_5),(0.3,y_6)}

Find Cartesian product represented by the relation R=X×Y Consider fuzzy set Z = {(0.3,x_1),(0.6,x_2),(0.7,x_3),(0.9,x_4),(1,x_5),(0.5,x_6)} find S = Z ° R Using max-min composition and max-product composition

3. Explain the term fuzzy concentration, fuzzy dilation. Suppose following atomic term is given as

"Small" = $\{\frac{1}{0}+\frac{0.8}{10}+\frac{0.5}{20}+\frac{0.3}{30}+\frac{0.1}{40}\}$ for this atomic term find membership functions for the following phrases

a] very small b] slightly Small

4. Describe important notation for representing fuzzy set and different fuzzy membership functions.
5. Design fuzzy controller for washing machine where input is dirt and grease and output is wash time.

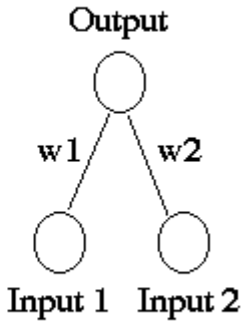
Assignments

ASSIGNMENT 1 (DATE : 9th FEB 2015)

:Single layer and multilayer perceptron:-

Q1. Apply the perceptron learning rule to solve the AND problem for w_1= -0.5, w_2 = 0.5, and θ= 1.5.

Input 1	Input 2	Output
1	1	1
1	0	0
0	1	0
0	0	0



Q2. Explain how to solve XOR problem.(Assume suitable data)

ASSIGNMENT 2 (DATE : 13th March 2015)

-:Fuzzy logic and fuzzy system:-

Q1. Design fuzzy controller for train to control break power according to speed and distance.

Q2. Design Fuzzy controller for fan regulator to control fan speed according to temperature.

PVPP'S

College Of Engineering

ELEC

FH 2015

ELECTRONIC PRODUCT DESIGN

Mrs.GOMATHI.M

Subject Plan

GROUP NAME	**: Electronic circuits design**
COURSE TITLE	**: Electronic Product Design**
COURSE CODE	**: Elective**
SEM	**: VIII (FH 2015)**
PRE-REQUISITE	: Electronic devices and circuits design,Digital circuits and design.

RATIONALE

This subject requires the student to know about basic knowledge of electronic circuits and devices and PCB layout designing.

Product design – the process of defining all of the companies product characteristics

- Product design must support product manufacturability (the ease with which a product can be made)
- Product design defines a product's characteristics of:
  - appearance, materials, and dimensions.

OBJECTIVES :

1. To cover product design and development stages and total coverage of product assessment by introducing the basics of reliability and quality of electronic product.

2. To discuss the various modes and causes of failure. To recognize the environmental effects on product development.

3. To study the power supply considerations, its design as per the considerations. To study the effects of noise and measurement and measures to reduce the noise.

4. To recognize the need of grounding and shielding for the products and to study different grounding and shielding techniques.

5. To understand the basic PCB designing rules. To study component assembly and testing of assembled PCB.

6. To study the automation technique(computer aided design) in PCB design. To study soldering techniques, study of packages for discrete devices and ICs, IC reliability issues.

7. To introduce high speed PCB design techniques, to recognize the parasitic elements in high speed PCBs its calculations and to discuss the points to be considered for designing high speed PCBs design.

8. To study the mounting and testing for multilayer PCB.

9. To study logic analyzer, spectrum analyzer, network analyzer, its architecture and operation with its functioning.

10. To recognize different types of scopes viz. oscilloscope, DSO, MSO its operation and trigger modes.

11. To discuss signal integrity issues, use and limitations of different types of analysis like Monte Carlo Analysis.

OUTCOMES :

1. Understandings of the different stages in product development and different types of parameters and requirements need to be considered while developing product.
2. Estimating power supply requirement which also called as power supply sizing and understanding the importance of grounding, shielding in product design phase also its different techniques.
3. Understanding the PCB design techniques with high speed PCB design, multilayer PCB and its testing.
4. Understanding of operation of logic, network and spectrum analyzer along with its operation.
5. Understand and analyze the different phases of software design and testing and debugging of the developed software and understanding of Simulators, Emulators and compilers etc.
6. Understand the EMI and EMC of the product developed and its importance while designing any product.
7. Analyzing the importance of documentation in product development.

LEARNING RESOURCES: -

RECOMMENDED BOOKS:

1.Electronic Product Design, R.G.Kaduskar, V.B.Baru,Wiley India

Reference Books :

1) Printed Circuit Board design and technology – Walter C Bosshart Tata McGraw Hill.

2) Handbook of Printed Circuit manufacturing – Raymond H. Clark

3) Electronic testing and fault diagnosis – G.C.Loveday, Ah wheeler Publication, India.

4) Electronics Engineers reference book 5th Edition – Edited by F.F.Mazda Butterworths Publication Co., UK

5) Principles of reliable Soldering Techniques, Sengupta R., New Age

International.

COURSE MATERIALS MADE AVAILABLE

4. Course instructional objectives & outcomes
5. Syllabus
6. Chapterwise Question Bank

Evaluation :

Theory Exam	100 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Expt. No.	Name of the Experiments
1	To calculate gain error due to resistance tolerance in an instrumention amplifier.
2	To study AC analysis of circuit
3	To prepare the specifications for DC power supply
4	To study the fault finding on OP-AMP using voltage regulator
5	Testing and measurement of 2 signal using DSO of given circuit
6	Temperature measuring circuit
7	To study the characteristics of HPF over Low to high frequency using spectrum analyzer.

Chapterwise Plan

Subject Title: Electronic product design

Chapter No. : 1

Chapter Name : Product Design and Developement

Approximate Time Needed : 12 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction, an overview of product development and product assessment.
2	Pilot production batch, concept of availability, screening test.
3	Environmental effects on reliability, redundancy.
4	Failsafe system, Ergonomic and aesthetic` design considerations.
5	Packaging and storage
6	Estimating power supply requirement(power supply sizing), power supply protection devices.
7	Noise consideration of a typical system
8	Noise in electronic circuit
9	Measurement of noise.
10	Grounding, shielding and guarding techniques.

11	Enclosure sizing and supply requirements and materials for enclosure.
12	Thermal management and its types

Objectives:

1. Review the main activities of performing a feasibility
2. study and selecting an optimum concept.
3. Discuss the main stages of designing and manufacturing a product.
4. Discuss the main activities involved in testing and refining
5. a new product and then launching and selling it.
6. Analyze the environmental issues that are involved in
7. making a product and in retiring it.
8. Explain the concepts of life cycle cost

Lesson Outcome:

Students will able to

1. Solve specific problems independently or as part of a team
2. Manage a project from start to finish

3. Work independently as well as in teams
4. Define, formulate and analyse a problem.

Model Questions:

Q.1 The failure rate per hour of a certain electronics product is given by $0.02\ (1+30e^{-2t}+e^{-t/20})$. Find the unreliability of the product at t= 104 hours.[May-11(5)]

Q.2 What are the different types of transient suppressors? Discuss the selection criteria for the same.[May-11(10)].

Q.3 Explain the bathtub curve for reliability.[May-11(5)], [Dec-12(5)], [May-13(5)].

Q.4 Justify availability and reliability are interrelated by maintainability.[May-11(5)].

Q.5 Define MTBF, MTTF, FR, Reliability.[Dec-11(5)], [May-13(5)].

Q.6 A transistor with VCE=20V and IC=1A has 1^0C/W junction to case thermal resistance if the value of QCS=0.4^0C. Calculate thermal resistance for heat sink that will keep maximum junction temperature at 90^0C, when the ambient temperature is 25^0C.[Dec-11(5)].

Q.7 Explain : (i) Grounding, (ii) Shielding. [Dec-11(10)].

Q.8 Explain the Bathtube curve for reliability indicating all its region. Also explain how failures are reduced prior to shipment of the product. [Dec-11(10)].

Chapterwise Plan

Subject Title: Electronic product design

Chapter No. : 2

Chapter Name : PCB DESIGNING

Approximate Time Needed : 12 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
13	Layout PCB sizes, Layout general rules and parameters.
14	Recommendations for decoupling and bypassing, design rules
15	digital circuit PCB and analog circuit PCB.
16	Noise Generation
17	Supply and ground conductors, Multilayer boards.
18	Component assembly and testing of assembled PCB
19	Bare board testing, component assembly technique
20	Automation and computers in PCB design, computer aided design and design automation.
21	Soldering techniques solder ability testing, study of packages for discrete devices and ICs, IC reliability issues
22	Parasitic elements, calculations of parasitic elements in high speed PCBs
23	High speed PCB design and points to be considered for designing the high speed PCBs.
24	Mounting in presence of vibration, SMD assemblies. Board layout checklist, tests for multilayer PCB cable.

Objectives:

1. Getting acquainted with various component
2. Identifying components through visual check
3. Component Handling
4. Component Functions
5. Datasheet reading
6. Replacing a part with equivalent part
7. Part selection from Digi key
8. Selection of component for your design
9. Introduction to Smart designing – Online

Lesson Outcomes:

The student will be able to

1. Schematic CAD Software.
2. Board Layout CAD Software
3. Transfer and developing of artwork

Model Questions:

Q.1 Compare single sided, double sided and multilayer PCB. [May-11(5)][Dec-11(5)]

Q.2 Calculate the characteristics impedance of a twisted pair wire diameter 0.3mm; length of wire, l=5cm; separation between wire centers, S=1mm; relative permittivity, εr =2.5. [May-11(10)]

Q.3 Write short notes on:-
(i) SMD assemblies, (ii) Soldering methods.[May-11(10)] [May-13(5)]

Q.4 Calculate characteristics impedance for a strip line geometry when thickness of PCB Laminate is 1.6mm and relative permittivity is 3.2. The width of embedded track is 1mm and its thickness is 35 microns. Calculate the width of track of micro strip geometry that will result in 75Ω characteristics impedance for the same above parameters.

[Dec-11(10)] [May-13(5)]

Q.5. What factors should be considered while designing high speed PCB?

[May-11(10)] [Dec-11(10)]

Q.6. A PCB is to be designed for weather monitoring DAS. What should be considerations in PCB designing? [May-12(10)]

Q.7. What are impedance considerations in PCB design of TTL, CMOS and ECL ICs. [May-12(5)]

Q.8. Find the resistance of a conductor of 10cm length and 0.35mm wide if standard copper foil is used. Calculate % change in resistance if PCB is operated at 65^0. If α cu=0.0039 and ρ=1.7241 x 10^{-6}(at 20^0C) cm. [May-12(5)]

Q.9. Explain complex board testing method. [May-12(5)]

Q.10. Describe component mounting considerations. [May-12(5)]

Q.11. What should be the width of the track of a micro strip geometry that will result in 50Ω characteristic impedance when the PCB laminate thickness is 1.6mm and its relative permittivity is 4.2? Assume the thickness of the track to be 70 microns. [Dec-12(5)]

Q.12. What are different PCB design considerations for microprocessor based circuit? [Dec-12(10)]

Q.13. Explain the importance of component layout in PCB design. [Dec-12(5)]

Q.14. Give constructional features, advantages and disadvantages of multilayer PCB. [Dec-12(5)] [May-13(5)]

Q.15. What is crosstalk? How will you minimize it? [Dec-12(5)] [May-13(5)]

Q.16 Explain the main factors to be considered for signal conductors in high gain DC amp. [Dec-12(5)]

Q.17 What is the need of a PCB testing? Explain the following methods of PCB testing in detail:-

(i) In-circuit testing
(ii) Functional testing
(iii) Boundary scan testing
(iv) Complex board testing. [May-13(10)]

Q.18 A metal wire makes a rectangular loop with diameter of wire 0.1 inch, length of loop is 2 inch and breathe 3 inch. Find the inductance offered by a rectangular loop. If diameter of The wire is changed to 0.3 inch, what will be the new inductance. Comment on results. [May-13(6)]

Q.19. Explain bare board testing method. [May-13(5)]

Q.20 Discuss different types of IC packages. [May-12(5)]

Chapterwise Plan

Subject Title: Electronic product design

Chapter No. : 3

Chapter Name : Hardware Design and testing methods

Approximate Time Needed : 6 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
25	Logic Analyzer: Architecture, operation and use.
26	Spectrum Analyzer: Architecture, operation and use
27	Network Analyzer: Architecture, operation and use
28	Oscilloscope, DSO trigger modes, Examples using MSO.
29	Signal integrity issues.
30	Use and limitations of different types of analysis, Monte Carlo Analysis.

Objectives:

1.Be able to analyze capacitive and inductive first order circuits including transients, equivalent circuits, initial and final conditions, and differential equations.

2. Be able to analyze and design first and second order circuits using Laplace transforms.

3. Understand and able to use transfer functions, analyze their natural and forced responses and stability.

4. Be able to apply appropriate models to analyze and design the frequency response in electronic circuits.

4. Be able to design and analyze circuits incorporating operational amplifiers.

Lesson Outcomes:

1.Design, analyze and test electronic circuits implemented with linear IC's

2. Simulation of circuits and systems with SPICE software packages.

3. Specify, design and test active filter circuits.

4. Use available laboratory equipment for pulse and frequency response testing of designs.

5. Design and evaluate instrumentation amplifiers.

6. Design, evaluate and test nonlinear circuits (limiters, oscillators, etc).

7. Document all design and laboratory testing in the form of an engineering notebook.

Model Questions:

Q.1 Compare Network analyzer and Spectrum analyzer. [May-11(5)]

Q.2 Explain following terms in relation to the logic analyzer-(i) timing acquisition, (ii) state acquisition and also explain how logic analyzer can be used for debugging of address
and
data bus of microprocessor. [May-11(10)]

Q.3 What are various types of oscilloscope? Explain in brief DPO. [Dec-11(10)]

Q.4 What is Monte-Carlo analysis? Give application areas of it.
[May-11(5)] [Dec-11(10)] [May-12(5)] [Dec-12(5)] [May-13(5)]

Q.5 Write short notes on :- (i) Signal integrity
(ii) Oscilloscope probes. [Dec-11(10)]

Q.6 Explain in brief operation of logic analyzer. [May-12(10)]

Q.7 Explain how DPO differs from conventional oscilloscope. [May12(5)]

Q.8 Compare analog and digital oscilloscope. [Dec-12(5)]

Q.9 States various features of logic analyzer. [Dec-12(5)]

Q.10 Draw block diagram of super heterodyne spectrum analyzer and explain [Dec-12(5)]

Q.11 What is signal integrity? Justify the significance of signal integrity. [May-13(5)]

Q.12 Draw basic architecture of logic analyzer and explain its operation in detail. [May-13(10)]

Q.13 Explain the measurement of two signals of any analog circuit CRO with neat sketches. [May-13(6)]

Chapterwise Plan

Subject Title: Electronic product design

Chapter No. : 4

Chapter Name : Software Design and testing methods

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
31	Introduction, phases of software design and goals of software design
32	Methods of program flow representation.
33	Structured program construct, testing and debugging of a program.
34	Software design, Finite state Machine. Design to use assembly &/or High level language for software development.
35	Assembler, Compiler, Compiler design
36	Simulators, CPU simulators, Emulators.

Objectives:

4. Provide an understanding of the errors that arise in practical DSP systems due to quantization and use of finite word length arithmetic
5. Study the effect of errors on signal quality.
6. Study the effects of finite word length arithmetic in DFT algorithms and digital filters
7. Analyze the existence of limit cycles in digital filters;

Lesson Outcomes

1. Develop an information system using accepted software development processes.
2. Produce user applications using a specialized technology that builds upon fundamental software development practices.
3. Apply principles of human-computer interaction in the design of computer interfaces.
4. Analyze a problem and identify the appropriate data, hardware components and/or software requirements to develop a feasible solution.
5. Use current tools and practices that support the software documentation process.

Model Questions:

Q.1.What are the desirable features of assemblers and cross compilers? [May-11(5)]

Q.2. Explain with help a real life microprocessor based product how all the steps in software development are implemented. [May-11(10)]

Q.3. What are the rules for drawing ASM chart. [Dec-11(5)]

Q.4 Explain various phases of software design. [Dec-11(10)] [May-12(5)] [May-13(10)]

Q.5 What is ASM? Using ASM design lift controller. [May-12(10)]

Q.6 Describe methods of program flow representation. [May-12(5)]

Q.7 State benefits of using Top-Down approach in software structure diagram [Dec-12(5)]

Q.8 Design sequence detector to detect the sequence 011. [Dec-12(10)]

Q.9 Design sequence detector to detect the sequence 10010. [May-13(10)]

Chapterwise Plan

Subject Title: Electronic product design

Chapter No. : 5

Chapter Name : PRODUCT TESTING

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
37	Environmental testing for product.
38	Environmental test chambers and rooms. Test carried out on the enclosures.
39	Electromagnetic Interference(EMI) issues and Electromagnetic Compatibility testing.
40	Electromagnetic compatibility(EMC) with respect to compliance.
41	conducted emission tests(Time domain) Methods, Radiated emission tests.
42	Basics on standard used, Instruments specifications

Objectives:

The student will learn

1 Environmental testing.
2 Electromagnetic compatibility (EMC).
3 Basics on standard used.

Outcomes:

The students will

6. Understand the need of product testing
7. Gain knowledge of various standards
8. Appreciate the advantages and disadvantages of EMC and EMI

Model Questions:

Q.1 Explain how conducted and radiated EMI originates. Explain in details the established methods to control the effect of them. [May-11(10)] [Dec-11(10)]

Q.2 Specify with justification the choice of environmental tests to be carried out on following:-

(i) Washing machine (ii) Laptop (iii) UPS. [May-11(10)]

Q.3 Give the importance of CE certification and IP standard for electronic product. [May-11(5)] Dec-12(10)]

Q.4 Why it is necessary to conduct following tests on electronic product:-
i) Radiated emission (ii) Conducted emission (iii) Radiated susceptibility (iv) conducted Susceptibility. [Dec-11(10)]

Q.5 Explain significance of vibration testing of electronic product. [May-12(5)]

Q.6 Which environmental tests are to be carried out on the following product? Why it is necessary- (i) TV (ii) UPS (iii) Washing machine. [May-12(10)]

Q.7 Explain following tests of an electronic product:-

(i) Humidity test (ii) Vibration test (iii) Bump test. [Dec-12(10)]

Q.8 Compare conducted EMI and radiated EMI. [May13(5)]

Q.9 Specify the effect of temperature, vibrations and moisture on an electronic instrument and components. Which environmental tests should be carried out on the following products and why? Also clearly explain how and where are these tests carried?

i)Mobile phone (ii) Laptop. [May-13(10)]

Q.10 What are the factors to be considered during enclosure design? Explain significance of IP323. [May-12(5)]

Chapterwise Plan

Subject Title: electronic product design

Chapter No. : 6

Chapter Name : DOCUMENTATION

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
43	PCB Documentation: Specifying laminated grade, drilling details, PCB finish .
44	Tin, solder, gold, silver plating, hot air leveling and bare board testing. Understanding advantages and limitations of each.
45	Product Documentation: bill of materials, production test specifications
46	Case study for real circuit, interconnection diagram a case study, front and rear panel diagrams for selected product.
47	Manuals: Instruction or operating manuals. service and maintenance manuals.
48	Fault finding tree, software documentation practices- for C programmers, Assembly programmers with particular focus on development of programmed by several engineers simultaneously.

Objectives:

The student will learn

1. PCB documentation.
2. Product documentation.

3.Manuals

Lesson Outcomes:

The students will become cognizant with various Documentations.

1. Document system requirements and/or developing materials for clients in the proper use of hardware or software.
2. Students will work cooperatively and effectively in teams to accomplish a shared goal.
3. Analyze local and global information technology (IT) trends, while recognizing the influences of IT on cultural, economic, ethical, and legal issues and responsibilities.

Model Questions:

Q.1 Explain the different types of manuals for a electronic product. May-11(10)] [Dec-12(10)] [May-13(10)]

Q.2 Draw a fault finding tree for debugging faults in a dual power supply. [May-12(5)].

Q.3 Explain the contents of standard PCB documents in electronic product. [May-12(10)]

Q.4What is need of manual? Explain in detail the user manual for any user product. [Dec-12(10)]

Q.5 Which information exists in good PCB documents. [Dec-12(5)]

Q.6 State and explain various software documentation. [May-13(10)]

Assignments

ASSIGNMENT 1 (DATE : 9th FEB 2015)

1 .A transistor with VCE=20V and IC=1A has 1^0C/W junction to case thermal resistance if the value of QCS=0.4^0C. Calculate thermal resistance for heat sink that will keep maximum

2. Draw a sketch of front panel of a digital multi meter and explain how ergonomics and aesthetics design considerations are taken care of in the same.

3.What is the need of a PCB testing? Explain the following methods of PCB testing in detail:-i)In-circuit testing

ii)Functional testing

iii)Boundary scan testing

iv)Complex board testing.

4. Discuss different types of IC packages

5. What are different PCB design considerations for microprocessor based circuit?

6. What should be the width of the track of a micro strip geometry that will result in 50Ω characteristic impedance when the PCB laminate thickness is 1.6mm and its relative permittivity is 4.2? Assume the thickness of the track to be 70 microns.

7. A PCB is to be designed for weather monitoring DAS. What should be considerations in PCB designing?

ASSIGNMENT 2 (DATE : 13th March 2015)

1.Compare Network analyzer and Spectrum analyzer.

2.What is Monte-Carlo analysis? Give application areas of it.

3.Explain how DPO differs from conventional oscilloscope.

4. Draw basic architecture of logic analyzer and explain its operation in detail.

5. Explain the measurement of two signals of any analog circuit CRO with neat sketches.

6. Explain various phases of software design.

7. Explain with help a real life microprocessor based product how all the steps in software development are implemented

PVPP'S
College Of Engineering

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ELECTRO

FH 2015

ADVANCE NETWORK TECHNOLOGY

PADMABHUSHAN VASANTDADA PATIL PRATISHTHAN'S
SINCERITY SACRIFICE
SYSTEM 1990
COLLEGE OF ENGINEERING
Empower The Knowledge

Mrs. KHUSHBOO SINGH

Subject Plan

GROUP NAME	**: COMMUNICATION NETWORK**
COURSE TITLE	**: Advanced Networking Technologies**
COURSE CODE	**:**
SEM	**: VIII (FH 2015)**
PRE-REQUISITE	: Communication Network

RATIONALE

This second course in communication network group aims to make student familiar with data communication technologies. This course also covers how to use them to: Design, Implement, Operate, Manage enterprise networks.

OBJECTIVES :

21. To study the basic concept of networking fundamentals.
22. To emphasize on the performance & design consideration of optical network.
23. To analyze the various LAN & WAN technologies and ATM network.
24. To study the network design, security & network management & control.

OUTCOME :

18. To gain Knowledge of networking fundamentals.
19. Student will be able to analyze the performance & design the optical network.
20. To understand the LAN, WAN & ATM networks.
21. Understand the network design, security & management control.

LEARNING RESOURCES: -

RECOMMENDED BOOKS: -

13. Data Network Design by Darren Spohn, 3e McGraw Hill publications
14. Data Communication and Network Security by Carr and Snyder, McGraw Hill Publications
15. Communication Networks by Leon-Garcia and Indra Widjaja, 2e, Tata McGraw-Hill Publications.
16. Information Security by Mark Stamp and Deven Shah by Wiley Publications
17. Behrouz A Forouzan, Data communications and Networking 4th Edition, McGraw-Hill Publication.
18. William Stallings, Data Computer Communications, Pearson Education
19. Local Area Networks by Gerd Keiser, McGraw-Hill Publication.
20. Computer Networking by J. F. Kurose and K. W. Ross, Pearson Education
21. Eldad Perahita ,Next Generation wireless LANS, Cambridge Publication

COURSE MATERIALS MADE AVAILABLE

1. Course instructional objectives & outcomes
2. Syllabus
3. Chapter wise Question Bank

Evaluation :

Theory Exam	100 M
Oral	25 M
Term Work	25 M
Total	150 M

List of Experiments

Atleast 06 experiments based on the entire syllabus

Expt. No.	Name of the Experiments

1	Network Installation & Configuration of Network OS.
2	To study network commands in linux
3	To study different types of network protocol analyzer.
4	Installation & Configuration of FTP Server/Client.
5	To study firewall design
6	Installation & Configuration of HTTP Server/Client.
7	Study of Wireless LAN (Ad-hoc & Infrastructure network mode)
8	Telnet & SSH service.

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 1

Chapter Name : Networking Fundamentals

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Overview of Internetworking architecture models: The OSI model.
2	TCP/IP protocol suite
3	Addressing, IP versions subneting and supernating.
4	Internetworking Protocols and standards, Standards Organizations
5	Internet Standards, Connectors, Transceivers and Media converters.
6	Network interface cards and PC cards.
7	Repeaters, Hubs, Bridges, Switches, Routers and Gateways etc.
8	Hardware selection.

Objectives:

5. To enable the students to learn the fundamentals of communication network.
6. To learn internetworking architecture models, addressing, internetworking protocols and standards.
7. To know about internet standards, connectors, transceivers and media converters.
8. To learn various hardware devices and hardware selections for different application.

Lesson Outcome:

Students will able to

1. Learn the fundamentals of communication network
2. Understand the internetworking architecture models, addressing, internetworking protocols & standards.
3. Understand about internet standards, connectors, transceivers and media converters.
4. Know various hardware devices and hardware selections for different application.

Model Questions:

1. Explain subnetting & supernetting with example. How do the subnet mask & supernet mask differ from a default mask in classful addressing?
2. An organization is granted the block 211.17.180.0/24. The administrator wants to create 32 subnets. a) Find the subnet mask. b) Find the no. of addresses in each subnet. c) Find the first & last addresses in subnet 1. d) Find the first & last addresses in subnet 32.
3. What is the difference between a port address, a logical address, and a physical address?
4. How does information get passed from one layer to the next layer in the Internet model?

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 2

Chapter Name : Optical Networking

Approximate Time Needed : 06 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	SONET/SDH Standards
2	SONET/SDH devices
3	DWDM
4	Frame format of SONET/SDH & DWDM
5	DWDM Performance
6	DWDM design considerations

Objectives:

1. To know SONET/SDH standards and devices.
2. To emphasize on DWDM: frame format, performance and design consideration.

Lesson Outcome:

Students will able to

1. Learn SONET/SDH standards and devices

2. Understand DWDM frame format, performance & design consideration.

Model Questions:

1. With the help of a neat sketch explain DWDM.

2. What are the four SONET layers? Discuss the functions of each layer.
3. What is the relation between SONET and SDH? Why SONET is called a synchronous network?

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 3

Chapter Name : LAN & WAN Technologies & ATM

Approximate Time Needed : 10 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Wireless LANs technologies & IEEE 802.11 standard
2	FR concept, FR specifications, FR design and VoFR.
3	Performance & design consideration
4	The WAN Protocol: Faces of ATM, ATM Protocol operations. ATM Networking basics: Theory of Operations.
5	B-ISDN reference model, PHY layer, ATM Layer (Protocol model) and cell.
6	Descriptor and parameters, Traffic Congestion control, Traffic contract and QoS.
7	AAL Protocol model.
8	User Plane overview, Control Plane AAL & Management Plane.
9	Sub S3 ATM.
10	ATM public services

Objectives:

5. Understand the LAN & WAN Technologies and standards.
6. Learn the Frame concept, specification and design & their performance
7. Understand ATM: Protocol operation and networking basics.
8. Study B-ISDN reference model, PHY layer, ATM layer, AAL protocol model & ATM public services.

Lesson Outcome:

Students will able to

1. Understand the LAN & WAN Technologies and standards.
2. Know the Frame concept, specification and design & their performance
3. Learn ATM: Protocol operation and networking basics.
4. Know B-ISDN reference model, PHY layer, ATM layer, AAL protocol model & ATM public services.

Model Questions:

18. Distinguish between the ATM & frame relay.
19. Sketch the frame format of frame relay and explain address field. How it provides congestion control and quality of service.
20. How is an ATM virtual connection identified?
21. Briefly describe the issues involved in using ATM technology in LANs.

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 4

Chapter Name : Network Design

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Introduction
2	Network layer design.
3	Access layer design
4	Access network capacity
5	Network topology
6	Network hardware
7	Network design issues.
8	Completing the access network design.

Objectives:

1. To understand Network layer design.
2. To learn Access layer design & network capacity.

3. To know the Network topology and hardware.

Lesson Outcome:

Students will able to

3. Learn Network & Access layer design & design issue
4. Understand Access network capacity, topology & hardware.

Model Questions:

1. What do you mean by network layer design? Explain.
2. Short note on: access network capacity, and network topology.
3. Discuss the access network design.

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 5

Chapter Name : Network Security

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Security threats, safeguards, and design for network security.
2	DMZ & NAT.
3	SNAT & DNAT.
4	Port Forwarding
5	Proxy
6	Transparent Proxy.
7	Packet Filtering
8	Layer 7 Filtering.

Objectives:

1. To understand Security threats & safeguards.
2. To emphasize on design for network security.

3. To know the DMZ, NAT, SNAT, DNAT, port forwarding, proxy & packet filtering for enterprise network security.

Lesson Outcome:

Students will able to

1. Learn Security threats & safeguards.
2. Comprehend design for Network security
3. Know the DMZ, NAT, SNAT, DNAT, port forwarding, proxy & packet filtering for enterprise network security.

Model Questions:

1. Explain in brief port forwarding.
2. Discuss in brief proxy and transparent proxy.
3. Explain in brief packet filtering and layer 7 filtering.
4. Write short note on: Enterprise Network Security.

Chapterwise Plan

Subject Title: Advance Networking Technologies

Chapter No. : 6

Chapter Name : **Network Management and Control**

Approximate Time Needed : 08 hrs

Lesson Schedule :

Lecture No.	Portion covered per hour
1	Documentation
2	OAM & P
3	RMON
4	Designing a network management solution.
5	Monitoring and control of network activity.
6	Monitoring and control of network activity.
7	Network project management
8	Network project management

Objectives:

1. Learn how to manage a communication network.
2. Analysis the designing of network management solution

3. Know the monitoring and control of network activity.

Lesson Outcome:

Students will able to

1. Manage a communication network.
2. Analyze the design of network management solution.
3. Understand the monitoring & control of network activity.

Model Questions:

1. Discuss: designing of network management solution.
2. Explain in brief the monitoring & control of network activity.
3. What do you understand by network project management?

Assignments

ASSIGNMENT 1 (DATE : 9th FEB 2015)

1. How do the layers of TCP/IP model correlate to the layers of OSI model?
2. Explain in detail Repeaters, Hubs, Routers, Bridges, Gateway and Switches. Give examples of each hardware device?
3. Write short note on : a) Internetworking protocols b) Network interface cards and PC cards c) Standard organizations d) Internet Standards e) Connectors f) Transceivers g) Media converters
4. Give the SONET/SDH hierarchy in brief.
5. Write short note on: a) SONET hardware b) SONET Networks c) SONET Frame Format.

ASSIGNMENT 2 (DATE : 13th March 2015)

1. Write short note on: a) IEEE 802.11 b) VoFR c) B-ISDN reference model d) Frame relay e) ATM public services f) ATM layers.
2. Explain in detail AAL also describe the concept of VPI & VCI?
3. With suitable sketch, explain ATM cell format for user-network interface.
4. What do you mean by access layer design? Explain.
5. What are various security threats? Describe network security safeguards in detail.
6. Write short note on: DMZ, NAT, SNAT & DNAT.
7. With respect to network management explain the following: documentation, OAM & P and RMON.

B.E Electronics sem VIII Rev. / 22 May 2014

Elective II – Adv. Networking Technologies

QP Code : MV-19117

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is compulsory.
(2) Answer **any four** from remaining questions.

1. (a) Explain the strategies for transition from IPv4 to IPv6. **20**
   (b) Compare ubiquitous and hierarchical access in Access Network Design.
   (c) Compare IPv4 and IPv6
   (d) Explain frame format of Frame relay.

2. (a) Explain ATM cell format in detail and compare Frame velay and ATM. **10**
   (b) With a neat flowchart, explain how CSMA/CA is implemented in WLAN. Why CSMA/CD cannot be implemented in WLAN. **10**

3. (a) Explain the importance of DCF, PCF, NAV vector with respect to IEEE 802.11 bringing out the importance of the protocol. **10**
   (b) What are the hardware components of DWDM? Explain the technology with a neat diagram. **10**

VIII / R / Electronics / R

25 : 2nd half.12-shilpa(e)

Con. 9997-12. (REVISED COURSE) KR-4950

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1 is compulsory.**
(2) Answer any **four out of remaining six** questions.

1. Answer the following :– 20
   (a) Explain BSS and ESS as defined by 802.11 and also explain how 'hidden station' problem is overcome in 802.11.
   (b) Compare Frame relay and ATM.
   (c) Bring out the salient differences between TCP/IP and OSI Model.
   (d) What is the need for fragmentation in IPV4 ? How is it implemented ? Explain with an example.

2. (a) Explain IPV4 datagram format in detail. What are the strategies for transition from IPV4 to IPV6 ? Explain. 10
   (b) For the following Network Componets, bring out the functions of each · Hubs, Repeaters, Bridges Switches, Routers. 10

3. (a) Briefly explain subnetting and supernting, with an example. How do the subnet mask and supernet mask differ from a default mask in classful addresing ? 10
   (b) Explain the steps for completing the Access-Network design in detail. 10

4. (a) Differentiate between CSMA/CD and CSMA/CA. Why CSMA/CD is not implemented in WLAN ? With a neat process flow-chart, explain how CSMA/CA is implemented in WLAN. 10
   (b) Explain ATM cell format. Aslo describe the different functional layers of ATM and bring out the significance of AAL layer. 10

5. (a) Explain DWDM technology with a neat schematic diagram of DWDM architecture, bringing out the main functions of the DWDM system components. 10
   (b) Describe frame format of Frame Relay and explain how congestion control is implemented in frame relay. 10

6. (a) What is a firewall ? What are the capabilities and limitations of firewall ? Explain different types of firewalls, their advantages and weaknesses. 10
   (b) Explain the different security threats and safegaurds. 10

7. Write short notes on :– 20
   (a) RMON
   (b) SONET functional Layers
   (c) Differences between IPV4 and IPV6
   (d) Layer - 7 filtering.

12/12/11 BE ETRX VIII CRED
Advanced Networking Technologies

Hnd. half-11-S.G. 63

Con.6566-11. **(REVISED COURSE)** **MP-5179**

(3 Hours) **[Total Marks : 100**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Solve any **four** from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) What are the functions of Network Layer ? **5**
   (b) With help of a suitable sketch explain Optical Networking in brief. **5**
   (c) Explain frame relay in brief. **5**
   (d) Discuss the need of Network Security. **5**

2. (a) Explain in detail Repeaters, Hubs, Routers and Gateways. **10**
   (b) Explain in detail ATM Adaptation Layer (AAL). **10**

3. (a) What do you mean by Network Layer Design ? Explain. **10**
   (b) Discuss the various fields in IPv4 frame. **10**

4. (a) Describe Network Security safeguard in detail. **10**
   (b) With respect to Network Management explain the following :— **10**
   (i) Documentation
   (ii) OAM & P.

5. (a) Describe the various wireless LAN technologies. **10**
   (b) Explain in brief ICMP. **5**
   (c) With the help of a neat sketch explain DWDM. **5**

6. (a) Explain ATM cell format in brief. **5**
   (b) Compare and contrast Ubiquitous and Hierarchical access. **10**
   (c) Explain in brief Layer 7 filtering. **5**

7. Write short notes on following :— **20**
   (a) Subnetting
   (b) Remote Monitoring
   (c) Congestion Control
   (d) VoFR.