Sem III E.T. (rev) 31/05/14

A.E. I

QP Code : **NP-18628**

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions out of remaining **five**.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data if required and **mention** the **same** in answer sheet.

1. Solve any **five** :— **20**
   (a) Explain effect of temperature on characteristics of PN junction diode.
   (b) Why LC oscillators are preferred for high frequency applications ?
   (c) Find R_B and R_C for the circuit shown to obtain $V_{CE} = 5V$ and Ic = 2mA

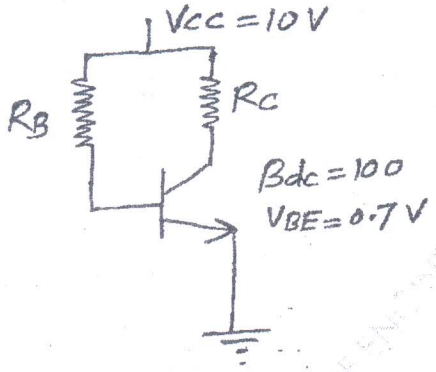

Fig. 1c

   (d) In n-channel MOSFET $V_{DS} = 5V$, $V_{GS} = 5V$, $V_{BS} = 0$, W = 10 μm, L = 5 μm, k'n=100 mA/V^2 and $V_{TO} = 1V$. Calculate its drain current for channel length modulation factor λ of 0 and 0·25 V^{-1}.
   (e) Draw and explain small signal hybrid-Pi model of BJT including early effect.
   (d) Differentiate between BJT and MOSFET.

2. (a) Find I_{CQ} and V_{CEQ} for the circuit shown in **figure 2a** if β = 100 **10**

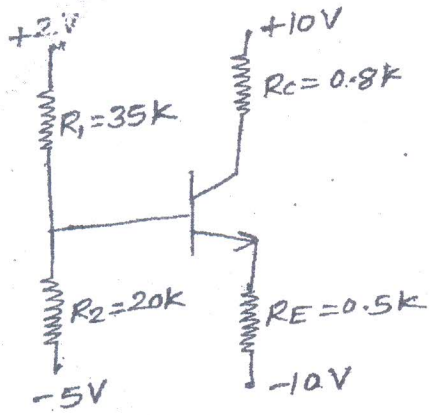

Fig 2a

[TURN OVER

(b) Draw and explain energy band diagram of MOS capacitor in accumulation, depletion and inversion region. 10

3. (a) Draw and explain working of transisterized Wien Bridge Oscillator. 10
   (b) The JFET shown in **figure 3b** has parameters $I_{DSS} = 8mA$ and $V_P = -4V$. Determine V_G, I_{DSQ}, V_{GSQ} and V_{DSQ}. 10

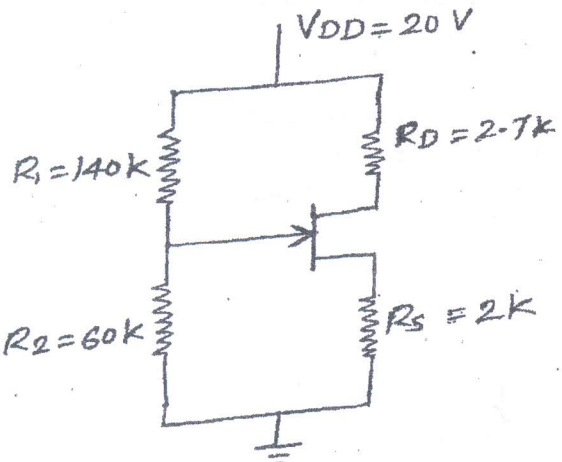

Fig 3b

4. (a) For the common gate circuit shown in **figure 4a**, the NMOS transistor parameters are $V_{TN} = 1V$, $kn = 3\ mA/V^2$ and $\lambda = 0$. 10
   (i) Determine I_{DSQ} and V_{DSQ}
   (ii) Calculate gm and ro
   (iii) Find the small-signal voltage gain $Av = \frac{v_0}{v_i}$. Assume Cc_1 and Cc_2 acts as short circuit for small-signal analysis.

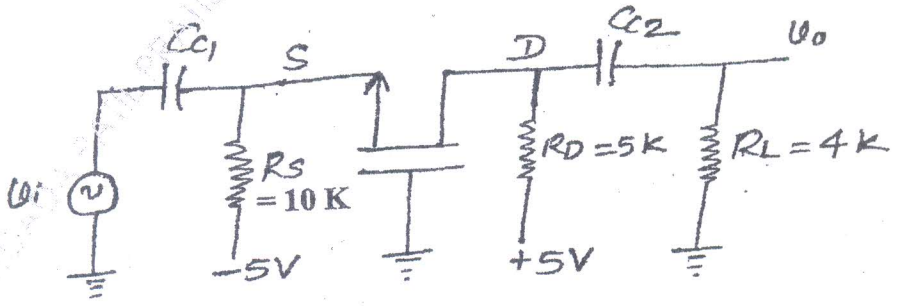

Fig 4a.

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(b) The parameters of the transistor in the circuit shown in **figure 4b** are $\beta = 100$ and $V_A = 100$ V. **10**

(i) Determine the dc voltages at base and emitter terminals.

(ii) Find Rc such that $V_{CEQ} = 3{\cdot}5$V and

(iii) Assuming C_c and C_E act as short circuit, determine small-signal voltages gain

$$Av = \frac{v_0}{v_s}.$$

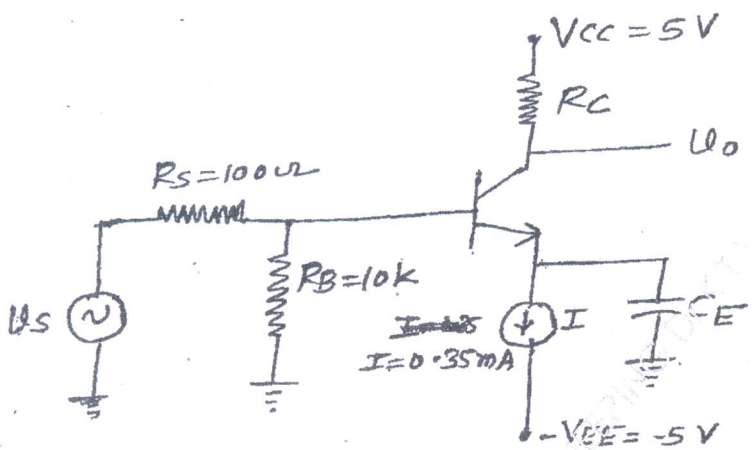

Fig 4b.

5. (a) Derive expression for voltage gain of NMOS source follower circuit. **8**

(b) For the common base amplifier shown in **figure 5b**, derive expression for voltage gain, current gain, input resistance and output resistance using hybrid-π model. **12**

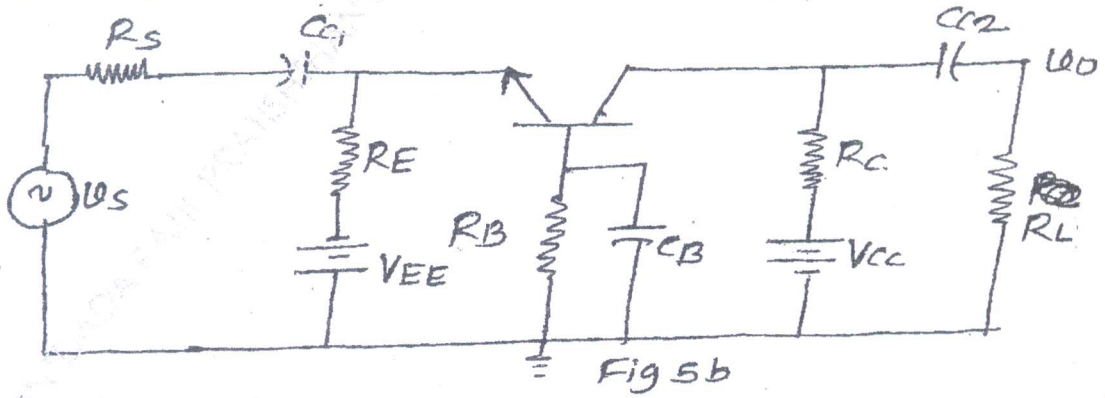

Fig 5b

6. Write short notes on any **three** :— **20**

(a) Series and shunt clippers

(b) Twin-T oscillator

(c) MOSFET operation

(d) Construction and operation of varactor diode.

SE(ET) Sem. III
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28.5.14

QP Code :**NP-18690**

(3 Hours) [Total Marks : **80**

N.B. (1) Question No. **1** is **compulsory.**
(2) Out of **remaining** questions, attempt any **three** questions.
(3) Assume **suitable** additional data if **required.**
(4) **Figures** in brackets on the **right** hand side indicate **full** marks.

1. Explain the following :– **20**
   (a) For ECL and CMOS logic families define–
   (i) noise margin (ii) fan-in (iii) fan-out.
   (b) Compare Asynchronous and synchronous counter
   (c) Explain static RAM
   (d) Explain Master-Salve J.K Flip-flop.

2. (a) Perform following operation using 2's compliment method– **5**
   (i) $(28)_{10} - (42)_{10}$ (ii) $(52)_{10} - (-18)_{10}$
   (b) Prove the following using Boolean algebra. **5**
   $\overline{A}BC + A\overline{B}C + ABC + AB\overline{C} = AB + BC + CA$
   (c) Design 2 bit comparator. **10**

3. (a) Minimum the following using Quine Mc Clusky method. **10**
   $F(A, B, C, D) = \Sigma m(3, 4, 9, 13, 14, 15) + \Sigma d(5,6)$
   (b) Design synchronous counter using J. K flip-flop for the given sequence — **10**
   0 – 2 – 3 – 5 –7 – 0.

4. (a) Design following Boolean equation using 4 : 1 mux **5**
   $F((A, B, C, D) = \Sigma m(2, 4, 5, 7, 9, 11, 12)$
   (b) Compare EPROM and FLASH memories. **5**
   (c) Explain bidirectional 4 bit universal shift register. **10**

5. (a) Explain 3 : 8 decoder. **5**
   (b) Explain Mealey machine and Moore machine. **5**
   (c) Write VHDL code for 3 bit binary down counter. **10**

6. (a) Explain Architecture and features of FPGA. **10**
   (b) Implement Ex-OR gate using NAND **5**
   (c) Convert (118_{10}) in to (i) BCD (ii) Hexadecimal (iii) octal. **5**

Con. 11692-14.

S.E. (EXTC), Sem. III (CBSGS) 03/06/2014

EIM.

QP Code : NP-18729

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question **No. 1** is **compulsory.**
(2) Solve **any three** out of the remaining.
(3) Assume suitable data if necessary.

1. (a) Define transducer and explain the classification of transducer. **5**
   (b) Explain with diagram principle of operation of frequency selective wave analyzer. **5**
   (c) Write the applications of Q meter. **5**
   (d) Describe various types of sweeps used in CRO. **5**

2. (a) Explain the principal of operation of dual slope DVM. **10**
   (b) Explain with neat diagram working principle of LVDT. Give its applications. **10**

3. (a) Explain various types of errors in measurement in detail. **10**
   (b) Explain with example working of successive approximation type ADC. **10**

4. (a) Explain in detail "Resistance strain gauges." **10**
   (b) Compare the temperature transducers RTD, thermistors & thermocouples on the basis of principle, characteristics, ranges & applications. **10**

5. (a) Explain performance characteristics of D/A converters. **10**
   (b) Explain the significance of 3½ and 4½ digit displays. **10**

6. (a) Draw & Explain block diagram of digital storage oscillospcoe & mention the modes of operation of DSO. **10**
   (b) Explain electrodynamometer type of wattmeter. **10**

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Con. 12832-14.

SE (ET) Sem-III (Old)
DLD.
28.5.14

(OLD COURSE) **QP Code : MV-17948**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume suitable **data** if **required**.

1. (a) Find binary, octal and hexadecimal equivalent for the following numbers :— **4**
   (i) $(23)_4$ (ii) $(61)_{10}$
   (b) Perform the following subtraction using TWO's complement method :— **4**
   (i) $(11011)_2 - (10101)_2$ (ii) $(17)_{10} - (12)_{10}$
   (c) Explain how Hamming code can be used as error correction code. **4**
   (d) Express the following numbers in Gray code :— **4**
   (i) $(45)_{10}$ (ii) $(11010111)_2$
   (e) Draw AND, OR, NOT and Ex OR gates using NAND gates. **4**

2. (a) Design a lockout free Mod 10 Synchronous Up counter using MS-JK Flip Flop. **10**
   (b) Draw a Two input TTL NAND gate circuit. Discuss the operation and draw its transfer characteristics. **10**

3. (a) Convert SR Flip Flop to JK and JK Flip Flop to D. **10**
   (b) Find the reduced logical expression using Quine McClusky method. **10**
   $F(A,B,C,D) = \Sigma m(0,2,4,5,6,7,8,9,10,12,14)$.

4. (a) For the following function find the reduced expression in SOP form and implementusing NAND gates only :— **10**
   $F(A,B,C,D) = \Sigma m(0,1,2,3,5,7,10,13,15)$
   (b) Design full Subtractor using decoders. **10**

5. (a) Explain the following characteristics with respect to logic families :— **10**
   Propagation Delay, Noise margin, Current parameters, Fan in and Fan out
   (b) Implement $F(A,B,C,D) = \Sigma m(0,1,2,3,4,5,7,9.10,13,15)$ using — **10**
   (i) one 8 : 1 multiplexer and (ii) 4 : 1 multiplexers tree.

6. (a) Design a circuit which will convert 4 bit Binary numbers to Gray numbers. **10**
   (b) Use PAL to implement the following functions :— **10**
   $F_1(A,B,C,D) = \Sigma m(0,1,5,6,8,11,14)$
   $F_2(A,B,C,D) = \Sigma m(0,1,5,6,8,11,14,15)$

7. Write short notes on (any **four**) :— **20**
   (a) Weighted and unweighted codes and their applications
   (b) Digital comparator
   (c) Boolean Algebra
   (d) Shift Registers
   (e) Universal Properties of NAND and NOR gates
   (f) PLA.

Con. 11674-14.