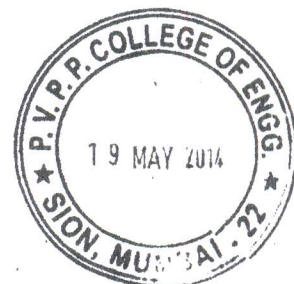QP Code : **MV-19968**

(3 Hours) [Total Marks : 100

N. B. : (1) Question No. 1 is **compulsory**.
  (2) Attempt any **four** questions from remaining questions.
  (3) Assume suitable data if necessary.

1. (a) Compare Butterworth, Chebyshev and Elliptic filter. 20
  (b) Compare FIR and IIR filter
  (c) Explain the concept of subband coding
  (d) Prove that symmetric and even length linear phase FIR filter have one compulsory zero at -1

2. Design digital lowpass Butterworth filter for the following specifications 20
  $0.92 \le |H(e^{jw})| \le 1 \qquad f \le 1200$ Hz
  $\quad |H(e^{jw})| \le 0.003 \quad f \ge 5000$ Hz
  Assume sampling frequency of 12000 Hz. Use Bilinear transformation technique for the design

3. (a) Explain the frequency transformation method in analog domain. 10
  (b) Explain the procedure of design of FIR filter using frequency sampling technique. 10

4. (a) Design digital FIR filter for the following specifications 10
  $Hd(e^{jw}) = 3e^{-j3\omega} \qquad 0.35\,\pi \le \omega \le 0.55\,\pi$
  $\qquad\quad = 0 \qquad\qquad$ otherwise

  Use Hanning window for the design.
  (b) What is an adaptive filter? What are its advantages? Which type of problems can 10
  be solved using adaptive filters.

5. (a) Explain weiner filter and its application 10
  (b) Explain Quadrature mirror filtering 10

6. (a) Explain with suitable example, the concept of polyphase interpolation. Compare 10
  it with single phase interpolation.
  (b) Explain Gibb's phenamenon and explain how it can reduced. 10

7. Write short notes on :— 20
  (a) FDNR and its properties
  (b) Switched capacitor filter
  (c) Higher-order filters
  (d) matched z-Transform.

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Con. 10559-14.

QP Code : **MV-20099**

(3 Hours) [Total Marks : 100

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Figures to the **right** indicate **full** marks.
(4) **Assume** suitable **data** wherever requried but **justify** it.

1. Answer the following :- 20
   (a) Compare symmetrical and asymmetrical semi-converter.
   (b) What is meant by voltage commutation and current commutation.
   (c) Compare series and parallel inverter.
   (d) What is four quadrant DC - drive.

2. (a) Explain sinusoidal pulse modulation as used in PWM inverter. 10
   (b) A load commutated chopper fed from 230 V d.c. source has a constant load 10
   current of 50 A. For a duty cycle of 0.4 and chopping frequency of 2kHZ.
   Calculate :-
   (i) Value of commutating capacitor.
   (ii) Average output voltage.
   (iii) Circuit turn off time for 1-pair of SCRs.
   (iv) Total commutation interval.

3. (a) Explain the working of a single phase series inverter with appropriate circut 10
   and waveforms.
   (b) Explain constant torque and constant power operation of separately excited 10
   DC motor. Give schematic diagram of control unit.

4. (a) A single plase fully controlled bridge with 230 V, 50 HZ supply feeds 10
   continuous ripple free current of 20A. If L_s = 2.5 mH.
   (i) Calculate overlap angle for firing angle 60°.
   (ii) What will be the new value of overlap angle for same firing angle if
   load is reduced by 50%.
   (b) Draw and explain the variable voltage and variable frequency control method 10
   for 3-phase squirrel cage induction motor. What is the significance of (V/F)
   ratio control.

5. (a) A single phase full converter is used to drive separately excited dc shunt 10
   motor with R_a =0.25 Ω. Motor rating are 220 V, 750 rpm, 50 A. If input
   voltage to converter connected to armature is 250 V a.c. 50 Hz.
   Calculate :-
   (i) Firing angle delay for 500 rpm at rated torque.
   (ii) Speed of motor for firing angle α = 60° at half load.
   (b) Explain the working of Jone's chopper with the help of various waveforms. 10

[**TURN OVER**

Con. 12250-14.

6. (a) Give the advantages of flyback converter compared to forward converter.   **10**
With the help of neat circuit diagram and wave form, explain the operation of
isolated forward converter.

(b) Using block diagram discuss different configurations of UPS.   **10**

7. Write short notes :-   **20**

    (a) Dual converter

    (b) Mc-Murray inverter

    (c) Four quadrant chopper.

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VLSI Design.

QP Code : MV-20169

(3 Hours)   [Total Marks :   100

N. B. : (1) Question no. **one** is compulsory.
      (2) Solve **any four** questions from remaining questions.
      (3) Draw neat diagrams wherever required.

1. Answer the following questions (write **any 4**).   20
  (a) The segregation coefficient of O_2 is 0.25. Find the concentration of oxygen in the silicon ingot at a fraction solidified of 0.3. The concentration of O_2 in the silicon at the top of the crystal is 12.5×10^{17} atoms/cm^3 at a fraction solidified of 0.1?
  (b) Draw the schematic, stick diagram of a NMOS depletion load inverter?
  (c) Explain what is pass transistor logic? Calculate the output voltage for the following circuits if Vdd = 5V and Vth = 1.5 V.
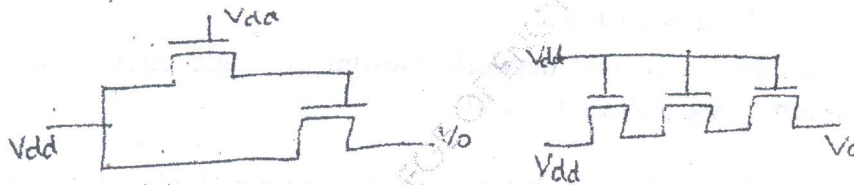
  (d) Define threshold voltage with equation and explain body effect?
  (e) State the difference between diffusion and ion implantation?

2. (a) With neat cross sectional diagram explain the process of CMOS fabrication using pwell process. Thus given the number of masks required.   10

  (b) Consider on aluminium - silicon dioxide - silicon MOS structure with the following parameters.   10
      $N_d = 2.5 \times 10^{14}$/cm^3
      $Q_{ox} = 10^{10}$ cm^2
      $T_{ox} = 650$ A$^\circ$
      $\phi_{ms} = -0.35$V
    Given $n_i = 1.45 \times 10^{10}$/cm^3, $\varepsilon_o = 8.85 \times 10^{-14}$
    $\varepsilon_{si} = 11.7$, $\varepsilon_{ox} = 3.97\varepsilon_o$
    Determine the threshold voltage of the device.

[**TURN OVER**

3. (a) Draw the circuit diagram of two input NAND gate using CMOS. Draw its   10
        stick diagram and layout using λ based rules.

    (b) State all types of inverters and compare them with their merits, demerits and   10
        applications.

4. (a) Determine pullup to pulldown ratio $\left(\dfrac{Zpu}{Zpd}\right)$ for an NMOS inverter driven   10

        by another NMOS inverter?

    (b) Explain latchup condition in CMOS in detail. What are the remedies to avoid   10
        latchup?

5. (a) A CMOS logic gate that implements the function.   10

        $F = X \cdot (Y + Z) + X \cdot W$

        is needed in a control network. Design the logic circuit and draw the stick
        diagram using Euler's method?

    (b) Design 4:1 MUX using CMOS transmission gate logic. Draw the stick diagram   10
        of the same design?

6. (a) Compare both the scaling methods? Show analytically how power dissipation,   10
        maximum operating frequency, current density and saturation current scale
        in terms of scaling factors?

    (b) Write switch level verilog code for a 2 input NAND gate. Using the module   10
        of NAND gate, design SR-Latch and write the switch level verilog code for
        the same.

7. Write short notes on **any two**:   20
        (i) Short channel effects in MOSFETs
        (ii) Comparision of burried and butting contacts.
        (iii) Semicustom and Full custom design.

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Con. 13089-14.